

**MILLIMETER-WAVE CMOS TRANSCEIVER FRONT-END
CIRCUITS FOR FUTURE ENERGY-EFFICIENT, LINEAR, AND
WIDEBAND COMMUNICATION SYSTEMS**

A Dissertation
Presented to
The Academic Faculty

by

Sensen Li

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2020

COPYRIGHT © 2020 BY SENSEN LI

**MILLIMETER-WAVE CMOS TRANSCEIVER FRONT-END
CIRCUITS FOR FUTURE ENERGY-EFFICIENT, LINEAR, AND
WIDEBAND COMMUNICATION SYSTEMS**

Approved by:

Dr. Hua Wang, Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. John Papapolymerou, Co-Advisor
Department of Electrical and Computer
Engineering
Michigan State University

Dr. John D. Cressler
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Andrew F. Peterson
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Gee-Kung Chang
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Kenichi Okada
Department of Electrical and Electronic
Engineering
Tokyo Institute of Technology

Date Approved: July 17, 2020

To my family and friends

ACKNOWLEDGEMENTS

Part of the journey is the end. When I first arrived at Georgia Tech, I was at my ignorant and impetuous age of 22. Now I am going to graduate, at almost 30, in hopes of becoming knowledgeable and mature. I have not only gained wisdom but forged my character in the process of pursuing my Ph.D. degree. Of course, none of my accomplishments could be possible without the help, support, and sacrifice from many great people. I want to express my sincere gratitude to them here.

Working in GEMS Lab under the supervision of Dr. Hua Wang for five years, I have been learning from the very best. I feel fortunate and grateful to work with him, and his passion, self-discipline, and wisdom has always kept me motivated. He is an excellent researcher that I look up to. His research philosophy has a great impact on me, and we always strive for true innovation and never satisfy with temporary success. As a professor, he not only thinks in a big picture but maintains a sharp technical capability. I remember when I first joined the group, Dr. Wang told me “we have a very high bar here”. Since then, I have constantly reminded myself to live up to the “bar” and expectations. I really appreciate the research environment Dr. Wang has created for us, which allows me to pursue the topics I am interested in with full support. Even after my graduation, I believe his influence will continue inspiring me for excellence throughout my career. I am proud to be a member of GEMS Lab.

I would also like to thank Dr. John Papapolymerou who first took me as a Ph.D. student. Under his supervision, I built my background in microwave engineering and gained first-hand experience in cleanroom fabrication, which greatly helps my later

research on RF and mm-Wave IC. There is an old Chinese saying that everything is much harder at the beginning. I am thankful for Dr. P's trust and patience on me when I first started my Ph.D. knowing nothing. I still remember the joy and encouragement when I saw the "WOW" Dr. P wrote on my exam after I got a nearly perfect score in his RF engineering class. I also do not forget that Dr. P did not blame me but appreciated my immediate report when I broke the D-band probe. Since then, I have never broken anything. His mentorship has guided me to an extent beyond the academic matters. I am proud to be a member of Mircotech Lab.

Special thanks are also given to my other thesis committee members: Dr. John D. Cressler, Dr. Gee-Kung Chang, Dr. Andrew F. Peterson, and Dr. Kenichi Okada. Their valuable suggestions and feedbacks have been very helpful to further improve my research.

Besides the professors, I feel very lucky and glad that I have met and worked with so many talented senior students, from whom I learnt a tremendous amount of technical knowledge and know-hows. More importantly, I always turn to them for help and advice whenever I run into a problem or dilemma. Therefore, I want to thank Dr. Taiyun Chi, Dr. Jong Seok Park, and Dr. Song Hu who are the first three Ph.D. students in our group. They laid down the foundation of our group as pioneers. I am deeply grateful to enjoy the legacy they left for the new generations of students and moreover, I view them as my models and have always been trying to achieve their level of success. I also would like to thank Dr. Spyridon Pavlidis, Dr. Christopher Barisich, Dr. Fan Cai, Dr. Aida Vera, Dr. Outmane Lemtiri Chlieh, and Dr. Wasif Tanveer Khan, who are my colleagues in Mircotech Lab. Spyros and Chris were so patient with my ignorant questions, and I learnt my first concept of cleanroom fabrication and PA designs from them. Fan and Aida taught me hand by hand

how to design antennas and filters, which helped me get a quick start at the initial stage of my Ph.D. study. I cherish my great memories with Outmane and Wasif, for their insightful technical advice and exotic delicious food they offered. I extend my sincere gratitude to Peter Song, Dr. Nelson Lourenco, Dr. Zach Fleetwood, and Dr. Chris Coen for their generous help on sharing their knowledge of different testing equipment, wire-bonder, dicing saw, and measurement setup with LN₂, which significantly facilitates the testing of my chips. Finally, I want to thank Dr. Yang Zhang, who has also been a great friend of mine. We share the same passion on a lot of things such as soccer and movie, and he always support and encourage me whenever I suffer a setback. I greatly appreciate the help from all my senior students at Georgia Tech.

When I came to a totally new environment alone, it is my great fellows from Zhejiang University that offered me help and made me feel accompanied and surrounded by friends. When I first arrived at Atlanta airport, Dr. Wenlei He and Dr. Yilin Liu picked me up. I still remember my first meal at Atlanta is at SoKongDong Tofu house with them. Dr. Nan Liu was a great leader of our ZJU-GT student community, and he put a lot of efforts to maintain our community. My first road trip is with Dr. Chen Jiang, and we drove all the way to Charlotte to cheer for our favorite team AC Milan. I want to thank every ZJUer (Dr. Yiming Kong, Dr. Zhou Lan, Dr. Ke Liu, Dr. Jilai Ding, Wei Shen, Wenjie Bao, etc.) that becomes a yellow jacket. It is my privilege to share the same journey with all of them.

My gratitude also goes to my peers and junior students in our group. I enjoy our technical discussions and group activities we participated in together. I want to thank Dr. Min-Yu Huang, Fei Wang, Doohwan Jung and Tso-Wei Li for the collaborations we had

during the years. I also appreciate the help from my junior students, Huy-Thong Nguyen, Tzu-Yuan Huang, Edgar Garay, Adam Wang, Amr Ahmed, David Munzer, Gregory Villiam Juneke, Sagar Kumashi, Jeongseok Lee, and Naga Sasikanth Mannem. I wish them great success in their future careers.

Many of my research projects require chip tape-outs and expensive equipment for testing. Without the generous support from our sponsors, my Ph.D. research could be much more difficult. Therefore, I want to express my appreciation to our sponsors, including Semiconductor Research Corporation (SRC), National Science Foundation (NSF), Defense Advanced Research Projects Agency (DARPA), Army Research Office (ARO), GlobalFoundries, Samsung Electro-Mechanics (SEMCO), Analog Devices Inc., Speedlink Technology Inc., Integrated Device Technology Inc. (now Renesas) and Intel.

In the journey of my Ph.D., I have been accompanied by many supportive and considerate friends. Especially, I want to thank Dr. Kexin Yang, Ye Chen, Xuanchang Shi, and Shuya Tong. During the most difficult period of my Ph.D., our friendship was the power that kept me going without loss of confidence in myself. My life in Atlanta is filled with the joyful times we spent together. I would also like to thank Hang Zhang, Yunyi Gong, Fanpeng Kong, Dr. Sylvain Le Liepvre, George Alexopoulos, and Dr. Wenjing Su for our shared memories at Georgia Tech.

Finally, and most importantly, I owe my deepest gratitude to my family. My parents offer me their unconditional love and support. I have been away from home since I was an undergraduate student. I am deeply indebted to my parents, and I hope to repay my parents for their love in the rest of my life. I never stop missing my grandparents who raised me.

They valued education and always hoped one day they could witness my Ph.D. graduation. I wish they could share my joy now. The most beautiful thing ever happened to me is that I met my fiancée Yiting Cui during my Ph.D. study. The years I spent with her at Atlanta is the happiest time of my life to now. Since she returned to China, we have been separated for almost four years. No words can describe how much I appreciate her understanding, support, and sacrifice. I would not get through my Ph.D. without her trust and company.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS	iv
LIST OF TABLES	xi
LIST OF FIGURES	xii
LIST OF SYMBOLS AND ABBREVIATIONS	xviii
SUMMARY	xx
CHAPTER 1. Introduction	1
CHAPTER 2. Multi-Feed Antennas for High-Efficiency Direct On-Antenna Power Combining	6
2.1 Introduction	7
2.2 Multi-Feed Slot Antennas at X-Band	10
2.2.1 Design and Implementation	10
2.2.2 Measurement	13
2.2.3 Conclusion	14
2.3 Dual-Feed Square Loop Antennas at Mm-Wave 5G Bands	16
2.3.1 Design and Implementation	16
2.3.2 Continuous Wave Measurement Results	27
2.3.3 Modulation Measurement Results	34
2.3.4 Conclusion	40
CHAPTER 3. A Mm-Wave Flip-Chip Packaged Chireix Transmitter with On-Antenna Outphasing Active Load Modulation	42
3.1 Introduction	42
3.2 Design Details of the 28-GHz Chireix Transmitter	45
3.2.1 Ideal Non-Isolating Power Combiners	45
3.2.2 On-Antenna Outphasing Active Load Modulation	47
3.2.3 Antenna Response to Outphasing	51
3.2.4 TX Circuit Schematic	53
3.2.5 Chireix Compensation	56
3.2.6 Hybrid Outphasing Operation	58
3.3 Measurement Results	59
3.3.1 Continuous-Wave Measurement	60
3.3.2 Wireless Modulation Test	64
3.3.3 PA Reliability Testing	66
3.4 Conclusion	68
CHAPTER 4. A Wideband Frequency Doubler with Transistor Multiport Waveform Shaping for 2nd Harmonic Enhancement and 4th Harmonic Suppression	70
4.1 Introduction	70

4.2	Theory and Design	71
4.3	Measurement Results	76
4.4	Conclusion	81
 CHAPTER 5. A Mm-Wave Current-Mode Inverse Outphasing Transmitter		
	Front-End: A Circuit Duality of Conventional Voltage-Mode Outphasing	82
5.1	Introduction	82
5.2	Conventional Voltage-Mode Outphasing Architecture and Its Limitations at Mm-Wave	84
5.3	Proposed Current-Mode Inverse Outphasing Architecture Employing a Parallel Power Combiner	94
5.4	Measurement Results	102
5.4.1	Continuous-Wave Measurement	102
5.4.2	Modulation Test	104
5.5	Conclusion	106
 CHAPTER 6. Multi-Feed Antenna and Electronics Co-Design: An E-Band Antenna-LNA Front-End with On-Antenna Noise-Canceling and Gm-Boosting		
6.1	Introduction	108
6.2	Circuit Modeling of Multi-Feed Antenna Systems	110
6.2.1	Multi-Feed Antennas in A Series Network Configuration	112
6.2.2	Multi-Feed Antennas in A Parallel Network Configuration	114
6.2.3	EM Verification of the Proposed Circuit Modelling	117
6.2.4	Modelling Multi-Feed Antenna Networks as On-Antenna Hybrid Series and Parallel Connections with Scaling	120
6.3	Multi-Feed Antenna and LNA Co-Design with On-Antenna Noise-Canceling and Gm-Boosting	122
6.3.1	On-Antenna Noise-Cancelling	122
6.3.2	On-Antenna G_m -Boosting	124
6.4	Design Details of the Antenna-LNA Front-End	126
6.4.1	Design Analysis for Signal Receiving	127
6.4.2	Design Analysis for Noise Cancellation	129
6.5	Measurement Results	133
6.5.1	Continuous-Wave Measurement	133
6.5.2	Over-the-Air Modulation Measurements	137
6.6	Conclusion	140
 CHAPTER 7. Conclusion		
		141
 REFERENCES		
		145

LIST OF TABLES

Table 3-1	Comparison with state-of-the-art mm-Wave silicon-based PAs/TXs	68
Table 4-1	Comparison with State-of-the-art mm-Wave Frequency Doublers	80
Table 5-1	Comparison Between Outphasing and Inverse Outphasing	96
Table 5-2	Comparison with State-of-The-Art Mm-Wave Silicon-Based PAs/TXs	106
Table 6-1	Comparison with State-of-The-Art E-band Silicon-Based LNAs/RXs	140

LIST OF FIGURES

Figure 2-1	(a) Power combining for an SFA using a passive network for impedance matching and power combining. (b) Antenna-array-based spatial power combining with conventional SFAs.	7
Figure 2-2	(a) Dipole-based MFA for direct on-antenna power combining meanwhile maintaining only one antenna footprint and the same antenna beamwidth. (b) Loop-based MFA that further demonstrates the generality of the MFA structure with enhanced bandwidth for high-speed and complex modulations at mm-Wave.	8
Figure 2-3	(a) DFA driven by two PAs in electronics-antenna integration. (b) DFA testing structure to mimic the scenario in (a).	9
Figure 2-4	(a) A conventional single-feed 0.5λ slot antenna and a 0.7λ slot antenna at f_0 . (b) The proposed multi-feed slot antenna schemes with a two-feed 0.5λ slot antenna and a three-feed 0.7λ shown as examples. (c) Theoretically calculated and EM-simulated driving impedances of the two-feed 0.5λ slot antenna vs. feeding locations.	11
Figure 2-5	(a) Fabricated samples. (b) The 3D EM model of the two-feed 0.5λ slot antenna. (c) The 3D EM model of the three-feed 0.7λ slot antenna with the equivalent circuit model of the matching networks.	13
Figure 2-6	Measured return loss and peak antenna gain versus frequency.	14
Figure 2-7	(a) (b) Measured and simulated radiation patterns of the two-feed 0.5λ slot at 10.4GHz. (c) (d) Comparisons between the measured radiation patterns of the two-feed and single-feed 0.5λ slot antenna.	15
Figure 2-8	(a) (b) Measured and simulated radiation patterns of the three-feed 0.7λ slot at 10.3GHz. (c) (d) Comparisons between the measured radiation patterns of the three-feed and single-feed 0.7λ slot antenna.	15
Figure 2-9	(a) Single-feed 1λ square loop antenna with its current distribution at f_0 as the reference design. (b) The dual-feed 1λ square loop antenna with its current distribution at f_0 .	16
Figure 2-10	EM-simulated (a) surface current distributions and (b) 3-D radiation patterns of the single-feed and dual-feed 1λ square loop antennas at 38.5 GHz.	17
Figure 2-11	Comparison in the (a) E-plane, (b) H-plane, and (c) S_{11} bandwidth between dual-feed and single-feed 1λ square loop antennas.	18

Figure 2-12	Simulated input impedance of the single-feed and dual-feed 1λ square loop antennas versus frequency.	18
Figure 2-13	Application example (a) one single PA drives the conventional SFA. (b) Two PAs are combined by the two-way Wilkinson power combiner and drive the SFA. (c) Two PAs drive the proposed DFA.	20
Figure 2-14	Feeding network of the proposed DFA.	22
Figure 2-15	(a) DFA with different ground geometries. (b) Radiation pattern comparison between the DFA with a large ground size and small ground size.	23
Figure 2-16	Input impedance of the DFA with a large and small ground plane.	24
Figure 2-17	The 3-D EM models of the (a) conventional SFA and (b) proposed DFA. (c) Layer stack-up and material used. (d) 3-D radiation patterns of the two antennas.	25
Figure 2-18	3-D radiation pattern of the DFA at 73.5 GHz using (a) 10-mil RO3003 and (b) 2-mil LCP. The simulated S_{11} of the DFA at 73.5 GHz using (c) 10-mil RO3003 and (d) 2-mil LCP.	26
Figure 2-19	Simulated (a) E-plane pattern, (b) H-plane pattern, and (c) S_{11} of the DFA on the substrates of three different thicknesses.	27
Figure 2-20	Photographs of the fabricated antenna samples using RO3003 substrates. The 38-GHz antennas use 10-mil-thick substrate and the 73-GHz antennas use 5-mil-thick substrate.	28
Figure 2-21	Antenna gain and pattern measurement setup for (a) 38.5-GHz antennas and (b) 73.5-GHz antennas.	29
Figure 2-22	Measured S_{11} for the dual-feed and single-feed 1λ square loop antennas (a) at 38.5 GHz and (b) at 73.5 GHz.	30
Figure 2-23	Measured broadside antenna gains for the dual-feed and single-feed 1λ square loop antennas (a) at 38.5 GHz and (b) at 73.5 GHz.	30
Figure 2-24	Measured absolute output power of both SFA and DFA in (a) E-plane and (b) H-plane.	32
Figure 2-25	Measured and simulated radiation patterns of the DFA and SFA (a) at 38.5 GHz and (b) at 73.5 GHz. (c) Comparison between the DFA and SFA at both 38.5 and 73.5 GHz.	33
Figure 2-26	38.5-GHz modulation test setup.	35

Figure 2-27	0.5GSym/s 16QAM and 64QAM modulation results at 38.5GHz of (a) SFA and (b) DFA.	36
Figure 2-28	The 1GSym/s (6Gb/s) 64QAM result of the (a) conventional SFA and (b) proposed DFA at 38.5 GHz.	36
Figure 2-29	Measured EVM of the DFA and SFA versus symbol rate for (a) 16QAM and (b) 64QAM at 38.5 GHz.	37
Figure 2-30	73.5-GHz modulation test setup.	37
Figure 2-31	0.5GSym/s 16QAM and 64QAM modulation results at 73.5 GHz of (a) SFA and (b) DFA.	38
Figure 2-32	1GSym/s (6Gb/s) 64QAM result of the (a) conventional SFA and (b) proposed DFA at 73.5 GHz.	39
Figure 2-33	Measured EVM of the DFA and SFA versus symbol rate for (a) 16QAM and (b) 64QAM at 73.5 GHz.	39
Figure 3-1	(a) Outphasing architecture, and (b) its vector representation.	42
Figure 3-2	Non-isolating outphasing combiner using (a) transformers and (b) $\lambda/4$ transmission lines.	43
Figure 3-3	Top-level schematic of the Chireix transmitter.	44
Figure 3-4	Proposed on-antenna outphasing power combiner.	47
Figure 3-5	Comparison of active load modulation between EM-simulated on-antenna outphasing network and ideal power combiner.	49
Figure 3-6	(a) Dual-feed antenna EM model. (b) Antenna radiation pattern at $\varphi = 0^\circ$. (c) Antenna input impedance and impedance bandwidth.	50
Figure 3-7	(a) Desired common-mode antenna impedance under packaging variations. (b) Differential-mode antenna impedance.	51
Figure 3-8	(a) Far-field nonlinearity characterization setup of the on-antenna combiner. (b) Simulated amplitude and phase response to outphasing operation.	52
Figure 3-9	(a) Schematic of the two-stage TX PA. (b) Schematic of TX mixer. (c) Simulated mixer LO and IF return loss.	54
Figure 3-10	(a) G_p and R_{out} of CS and cascode PA versus input power. (b) Performance comparison between CS and cascode PA in outphasing operation.	55

Figure 3-11	(a) Equivalent circuit for the two outphasing paths. (b) Chireix combiner efficiency at power back-off with zero source resistance (R_S). (c) Chireix combiner efficiency at power back-off with different R_S values.	57
Figure 3-12	Hybrid outphasing operation principle.	59
Figure 3-13	(a) Fully packaged Chireix TX module. (b) X-ray image for verification of flip-chip transition alignment. (c) Sub-TX die photograph. (d) PA standalone TS. (e) Back-to-back TS of OMN of PA TS.	60
Figure 3-14	(a) CW measurement setup. (b) Chireix TX performance over frequencies. (c) PA large signal behaviors at 28 GHz. (d) S-parameters of the back-to-back PA TS OMN. (e) PA TS large signal performance at 28 GHz.	61
Figure 3-15	Measured TX output spectrum.	63
Figure 3-16	(a) Nonlinearity characterization and modulation test setup. (b) Measurement results of 64-QAM at 6 and 15 Gb/s.	64
Figure 3-17	Chireix TX modulation performance versus bit rate with 64-QAM.	65
Figure 3-18	Measured modulation results at different directions with 6 Gb/s 64-QAM, demonstrating wide antenna FoV.	66
Figure 3-19	PA reliability test at P_{1dB} with P_{out} and I_{DC_PA} being monitored over 24 h ($P_{in} = -5$ dBm, $V_{dd} = 1$ V).	67
Figure 4-1	Comparison between (a) conventional push–push pair and (b) proposed multiport driven frequency doubler, illustrating current waveform reshaping for 4th harmonic suppression and 2nd harmonic enhancement.	71
Figure 4-2	EKV FET model used to mathematically analyze the current waveform in the conventional and proposed frequency doubler structures.	73
Figure 4-3	Top-level multiport driven frequency doubler schematic with wideband dual-resonance input 2 nd harmonic trap filter and the corresponding passive structures.	74
Figure 4-4	Simulation results of the (a) wideband input second-order harmonic trap and (b) its trajectory on Smith Chart, (c) broadband input matching, and (d) impedance seen by the doubler core (Z_L) at the output.	75

Figure 4-5	Die micrograph (core area: $370\ \mu\text{m} \times 270\ \mu\text{m}$).	76
Figure 4-6	Measured P_{out} and CG of the multiport driven frequency doubler (a) with fixed P_{in} and (b) at saturation.	77
Figure 4-7	Measured frequency doubler output power and dc power consumption versus input power at the output frequency of 60 GHz.	78
Figure 4-8	Measured drain efficiency η_D of the multiport driven frequency doubler over frequencies.	78
Figure 4-9	Measured averaged phase noise before (at 25-GHz input) and after (at 50-GHz output) the frequency doubling.	79
Figure 4-10	Measured fundamental signal rejection and large-signal S_{11} of the multiport driven frequency doubler.	79
Figure 4-11	Measured output spectrum of the multiport driven frequency doubler.	80
Figure 5-1	Outphasing architecture and its vector representation.	83
Figure 5-2	(a) Conventional voltage-mode outphasing architecture with a series power combiner. (b) Theoretical outphasing active load modulation.	86
Figure 5-3	(a) Conventional voltage-mode outphasing with nonzero output resistance. (b) Simulated power gain and output resistance of a CS and cascode PA core at 28GHz.	89
Figure 5-4	(a) Conventional voltage-mode outphasing with nonzero output resistance and Chireix compensation. (b) Theoretical φ - V_L relationship in ideal outphasing, and practical cases depicted by (11) and (16).	91
Figure 5-5	Theoretical outphasing efficiency η_{op} versus (a) φ and (b) PBO.	92
Figure 5-6	(a) Simulated P_{out} - φ dependence in an ideal case, and in outphasing with saturated linear (CS and cascode) PAs (OP w/ CS, and OP w/ Cas). (b) Simulated PAE and AM-PM versus PBO in both outphasing implementations with CS and cascode PAs.	94
Figure 5-7	(a) Proposed current-mode inverse outphasing architecture. (b) Effective load impedances seen by each PA path.	94
Figure 5-8	(a) Outphasing and (b) inverse outphasing active load modulation trajectory on Smith Chart (Γ_φ and $\Gamma_{-\varphi}$ are the PA output reflection coefficients at the phase-leading and phase-lagging path).	97

Figure 5-9	(a) P_{out} versus φ and (b) effective PA load resistance (R_p or R_s) in outphasing and inverse outphasing operation.	98
Figure 5-10	(a) Inverse outphasing architecture with finite PA output resistances. (b) Theoretical inverse outphasing efficiency versus PBO.	99
Figure 5-11	(a) Top-level circuit and building block schematic. (b) EM model of the output network and its simulated passive efficiency.	101
Figure 5-12	(a) Chip microphotograph of the inverse outphasing TX. (b) The CW and modulation measurement setup for output power and nonlinearity characterizations. (c) The TX large-signal performance at 29GHz. (d) The frequency response of the inverse outphasing TX.	103
Figure 5-13	(a) Demodulated 64QAM constellations and spectra at different modulation bandwidth. (b) EVM and ACLR of 64QAM versus modulation bandwidth. (c) Average output power and PA drain efficiency versus modulation bandwidth. (d) 16- and 256-QAM modulation testing results.	105

LIST OF SYMBOLS AND ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
AWG	Arbitrary Waveform Generator
BEOL	Back End of Line
CG	Common-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common-Source
CW	Continuous-Wave
DC	Direct Current
DE	Drain Efficiency
DFA	Dual-Feed Antenna
DLA	Dual-feed Loop Antenna
DPD	Digital Pre-Distortion
DUT	Device Under Test
EIRP	Equivalent Isotropic Radiated Power
EVM	Error Vector Magnitude
FBW	Fractional Bandwidth
FET	Field-Effect Transistor
FoV	Field of View
LCP	Liquid Crystal Polymer
LNA	Low Noise Amplifier
LUT	Look-Up Table
MFA	Multi-Feed Antenna

Mm-Wave	Millimeter-Wave
MIMO	Multiple-Input Multiple-Output
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PBO	Power Back-Off
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RX	Receiver
SFA	Single-Feed Antenna
SOI	Silicon-on-Insulator
SRF	Self-Resonant Frequency
T-line	Transmission line
TRX	Transceiver
TS	Test Structure
TX	Transmitter
VNA	Vector Network Analyzer

SUMMARY

To address the exponentially growing data-rate demand, it is envisioned that millimeter-wave (mm-Wave) will be extensively employed in 5G-and-beyond communication system for its broader spectra and proportionate increases of channel capacity. Viable mm-Wave transmitter (TX) front-end solutions are expected to support multi-gigabit per second spectrum-efficiency modulated signals, such as high-order quadrature amplitude modulations (QAMs). The corresponding large peak-to-average power ratios (PAPRs) of the high-order QAM and Orthogonal Frequency Division Multiplexing (OFDM) push the already stringent linearity-efficiency requirements on the deployed TXs/power amplifiers (PAs). On one hand, the TX/PA must exhibit excellent linearity over a large dynamic range to maintain the signal fidelity. On the other hand, the TX/PA should enhance its efficiency at power back-off (PBO) to minimize overall power consumption and thus alleviate thermal management. Such demands have stimulated extensive research on new TX/PA architectures to further advance the performance envelope at mm-wave. Feasible mm-Wave receiver (RX) front-end solutions should achieve high sensitivity and linearity while maintaining a wide bandwidth to handle high-speed and high-order modulated signals. A low RX noise figure (NF) and the resulting high RX sensitivity are essential to compensate the high path loss at mm-Wave in wireless communication. Moreover, massive multiple-input multiple-output (MIMO) and phased array architectures are extensively utilized to improve mm-Wave link performance and spatial diversity via beamforming. A high linearity RX implementation is required to avoid decorrelations among the MIMO/phased-array elements and mitigate intermodulation

distortions during concurrent multi-beams/streams receiving. My Ph.D. research aims to exploit new circuit architectures and techniques to address the mm-Wave transceiver (TRX) design challenges.

First, a multi-feed antenna structure is proposed to achieve direct on-antenna power combining with high efficiency. It eliminates the lossy power combining network at the output of PAs or TXs, boosting the total output power (P_{out}), equivalent isotropic radiated power (EIRP), and system efficiency. Different baseline antenna prototypes are demonstrated in a multi-feed fashion, showing the generality of the on-antenna power combining concept.

Secondly, by further leveraging antenna-electronics co-design, a 28GHz Chireix TX front-end with on-antenna outphasing active load modulation is implemented in a 45nm CMOS SOI process. The two phase-shifted sub-TXs are integrated with a dual-feed loop antenna (DLA) on package through flip-chip interconnects. In our proof-of-concept demonstration, the Chireix TX achieves $1.4\times$ PA drain efficiency enhancement at 6dB PBO compared to an ideal Class-B PA. In a wireless communication environment, the Chireix TX supports $>10\text{Gb/s}$ high-order QAM signals with high fidelity while maintaining high average efficiency.

Thirdly, we propose a frequency doubler topology utilizing transistor multi-port waveform shaping to increase the 2nd-order transconductance nonlinearity, suppress the output 4th and odd harmonics, and substantially boost the 2nd harmonic generation efficiency. Moreover, a broadband input 2nd harmonic trap as well as wideband input and output matching networks are implemented on-chip to achieve a $>60\%$ fractional

bandwidth (FBW) from 46 to 89GHz, making it favorable for various wideband/multi-band mm-Wave applications, such as 5G communication, E-band wireless backhaul, and hyperspectral mm-Wave imaging.

Next, we present a mm-wave TX front-end employing a new inverse outphasing architecture with current-mode PAs, unlocking outphasing applications at (high) mm-Wave. The conventional outphasing operation exhibits strong dependence on its voltage-mode driving source assumption and thus shows major limitations at mm-Wave. The proposed current-mode inverse outphasing architecture employs current-mode driving source and is inherently compatible with mm-wave linear PAs. Moreover, the conventional series outphasing combiner is replaced by a much simpler and low-loss parallel power combining scheme. As a proof-of-concept, a 28GHz TX front-end using cascode PAs based on inverse outphasing architecture is implemented, demonstrating state-of-the-art continuous-wave (CW) and modulation performance.

The last technical part of this dissertation introduces an antenna-RX co-designed example, demonstrating unique on-antenna low noise amplifier (LNA) noise cancellation and g_m -boosting techniques. We also propose equivalent circuits to model multi-feed antenna systems and elucidate on-antenna signal processing operations. As a proof of concept, we implement an E-band antenna-LNA front-end and explore the interactions among a common-gate (CG) LNA path, a common-source (CS) LNA path, and a pair of near-field coupled folded slot antennas for on-antenna noise-cancellation and g_m -boosting. In the measurements, a true Y-factor radiation method is introduced as a new and additional approach to measure the NF of the on-chip multi-feed antenna and LNA/RX integration.

CHAPTER 1. INTRODUCTION

“I was gratified to be able to answer promptly, and I did. I said I didn't know.”

— Mark Twain

“Grab every opportunity to take responsibility and do things for which you are unqualified.”

— Freeman Dyson

There has been an exponential growth of data-rate demand for modern wireless communication over the past decades. Such explosion in wireless data traffic is a consequence of the rapid growth of smartphones, tablets and other portable devices that transmit and receive ZettaBytes of data every year. This trend continues with the upcoming 5G wireless systems that will leverage mm-Wave spectrums with large bandwidth and the resulting proportionate increase of channel capacity. The 5G mobile and point-to-point communications will pose stringent demands on wireless mm-Wave TRXs, in terms of radiated power, operation bandwidth, energy efficiency, sensitivity and linearity.

Complementary metal-oxide-semiconductor (CMOS) technology offers unparalleled computation resources and integration level. My Ph.D research utilizes the powerful CMOS platform to explore new circuit techniques and architectures aiming to address the challenges in the next-generation communication systems. Though the time of my Ph.D. research at Georgia Tech, I have been working on feasible mm-Wave TRX front-end solutions to enable high-power, energy efficient, and wideband transmission, with low-noise and high-linearity receiving. The important contributions of this dissertation is summarized in the following.

1. We propose a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with direct on-antenna power combining and increases the total radiated power of a wireless transmitter with high efficiency.
2. Based on the proposed on-antenna power combining, an antenna-level outphasing active load modulation is further exploited. As a proof of concept, a 28GHz flip-chip packaged Chirex transmitter front-end is demonstrated, achieving state-of-the-art PA efficiency at both peak P_{out} and PBO among silicon-based designs.
3. To increase the device harmonic generation, we propose transistor multi-port waveform shaping, based on which, a wideband high-efficiency mm-Wave frequency doubler is implemented. A theoretical model is built to predict the transistor current waveform that is further engineered to enhance the desired 2nd harmonic and suppress the unwanted 4th harmonic. The prototype demonstrates the highest efficiency with a large instantaneous bandwidth in silicon.
4. A new current-mode inverse outphasing architecture is proposed to overcome the bottleneck that limits the (high) mm-Wave application of conventional outphasing architecture, replacing the conventionally required voltage-mode driving sources and series output power combiner. A unique circuit duality relationship is discovered from our theoretical analysis, with derived mathematical closed-form equations describing the (inverse) outphasing operations and achievable efficiency.
5. To extend our proposed antenna-electronics co-design methodology to RX implementations, we implement an E-band LNA co-designed and co-integrated

with an on-chip multi-feed antenna for antenna-level LNA noise-canceling and gm-boosting. Moreover, we also introduce a theoretical analysis framework on generic multi-feed antenna systems and classify them into three fundamental network configurations: series, parallel or hybrid networks. The equivalent and generalized circuit models of various multi-feed antenna systems with on-antenna passive voltage/current/impedance transformation are further proposed to offer circuit design insights and facilitate future antenna-circuits co-design innovations.

The remainder of this dissertation is organized as follows.

Chapter 2 introduces the proposed multi-feed antenna for high-efficiency on-antenna power combining. A multi-feed slot antenna and a multi-feed square loop antenna are used as examples for theoretical study and experimental demonstration. The driving impedance for a multi-feed antenna is derived analytically, and circuit models based on ideal transformers are developed to describe its on-antenna power combining capability. The multi-feed slot antenna and multi-feed square loop antenna are implemented on the PCB at X-band and potential 5G mm-Wave bands, together with conventional single-feed antennas as reference designs. Measurement results are shown to verify the on-antenna power combining of the proposed multi-feed antennas.

Chapter 3 presents a flip-chip packaged 28-GHz Chireix outphasing TX for PA efficiency enhancement at both peak P_{out} and PBO. We investigate the possibility of employing a multi-feed antenna as a multi-port passive network to perform outphasing active load modulation. As a proof of concept, an outphasing TX architecture is proposed by leveraging a DLA to achieve high efficiency transmission of wideband complex

modulated signals. Theoretical analysis and simulation are both performed proving that the proposed DLA is electrically equivalent to an ideal differential series non-isolating power combiner, enabling superior on-antenna outphasing operation. Therefore, multi-functional signal processing is achieved in a single-loop antenna footprint, including high-efficiency on-antenna power combining, outphasing active load modulation, and mm-Wave signal radiation. Moreover, unlike conventional spatial vectorial combining techniques (e.g., spatial IQ or spatial outphasing), the antenna-level signal processing preserves the wide antenna unit field of view (FoV) and is particularly suitable for array or MIMO applications.

A wideband high-efficiency frequency doubler leveraging transistor multi-port waveform shaping is presented in Chapter 4. Unlike the conventional push-push pair with grounded source terminals, the voltage swings on both the gates and sources of the proposed doubler are optimized with proper amplitude and phase. The resulting drain current bifurcation is greatly reduced, leading to suppression of the undesired 4th harmonic and significant enhancement of 2nd harmonic current. We also adopt the EKV FET model to provide a mathematical analysis of the current waveform shaping in both conventional and proposed topologies, which agrees well with the circuit schematic simulations. Broadband fundamental matching and a dual-resonance 2nd harmonic trap filter are implemented, which together guarantees the wideband frequency doubling performance.

Chapter 5 presents a mm-wave TX front-end employing a new inverse outphasing architecture with current-mode PAs. The proposed approach breaks through the bottleneck in the conventional voltage-mode outphasing architecture. Theoretical study is first conducted, revealing the strong dependence of the conventional outphasing operation on its voltage-mode driving source assumption. Consequently, it exhibits major limitations at

mm-wave, since efficient and linear mm-wave PAs often behave as current sources. To address this challenge, we propose a current-mode inverse outphasing architecture that employs current-mode driving source and is inherently compatible with mm-wave linear PAs. Moreover, the conventional series outphasing combiner is replaced by a much simpler and low-loss parallel power combining scheme. Closed-form mathematical expressions are derived for both the outphasing and inverse outphasing operations, including the active load modulation, Chireix compensations, and outphasing efficiency, which fundamentally explains the limitations of the conventional approach and the advantages of the inverse outphasing architecture. Further theoretical analysis discovers a circuit duality relationship between outphasing and inverse outphasing architectures, offering unique circuit intuitions.

In Chapter 6, we present an antenna-RX co-designed example, demonstrating an E-band LNA with an on-chip multi-feed antenna for antenna-level LNA noise-canceling and g_m -boosting. Equivalent circuits are also proposed to model multi-feed antenna systems and elucidate on-antenna signal processing operations. As a proof of concept, we propose an antenna-LNA co-designed architecture and explore the interactions among a CG LNA path, a CS LNA path, and a pair of near-field coupled folded slot antennas for on-antenna noise-cancellation and g_m -boosting. In the measurements, a true Y-factor radiation method is introduced as a new approach to measure the NF of the on-chip multi-feed antenna and LNA/RX integration. Then, we perform the conventional sensitivity-based NF measurement. Both measurements show accurate and consistent NF characterization at high mm-Wave.

Finally, Chapter 7 summarizes this dissertation.

CHAPTER 2. MULTI-FEED ANTENNAS FOR HIGH-EFFICIENCY DIRECT ON-ANTENNA POWER COMBINING

This chapter presents a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with on-antenna power combining and increases the total radiated power of a wireless transmitter. The driving signals at the multiple antenna feeds are scaled properly in amplitude and phase, so that they collectively synthesize the desired on-antenna current/voltage distribution and achieve the desired far-field radiation pattern. The proposed multi-feed antenna offers flexibility to optimize the antenna driving impedances based on the locations of the feeds. It also simplifies the passive impedance-matching and power-combining networks between the antenna feeds and the transmitter outputs, substantially increasing the total transmitter power efficiency. Most importantly, the proposed multi-feed antenna achieves on-antenna low-loss power combining, which, compared with antenna-array based spatial power combining, does not suffer from narrowed beam-width or enlarged antenna panel size.

As proof of concept, multi-feed slot antennas and multi-feed square loop antennas are designed and characterized on PCB at both X-band and potential 5G mm-Wave bands. Conventional single-feed slot antennas and single-feed square loop antennas are also implemented as reference designs. Well matched antenna gains and radiation patterns between the proposed multi-feed antennas and the conventional single-feed antennas are achieved in the measurements, demonstrating the on-antenna power combining of the proposed multi-feed antennas without distorting the far-field radiation patterns.

2.1 Introduction

Most existing antennas are one-port or single-feed radiators, which poses a fundamental design challenge for the wireless transmitters on their achievable output power and efficiency. This is particularly true for low-cost silicon processes with limited supply voltages. For high-power applications, outputs from multiple transmitters or power amplifiers need to be combined at the single-feed port of the antenna using passive power-combining networks as shown in Figure 2-1(a). However, large impedance-transformation ratio is often required for these passive networks to down-scale antenna impedance to the desired load-pull impedance of the high-power PAs [1], which results in high passive loss and limited operation bandwidth. Alternatively, antenna array can be implemented to spatially combine the power at the far field [Figure 2-1(b)]. But large-scale array implementation occupies a large array panel area and results in a much narrower beamwidth [2]. Such a narrow beamwidth complicates the transmitter/receiver alignment and poses various challenges particularly for dynamic and mobile applications.

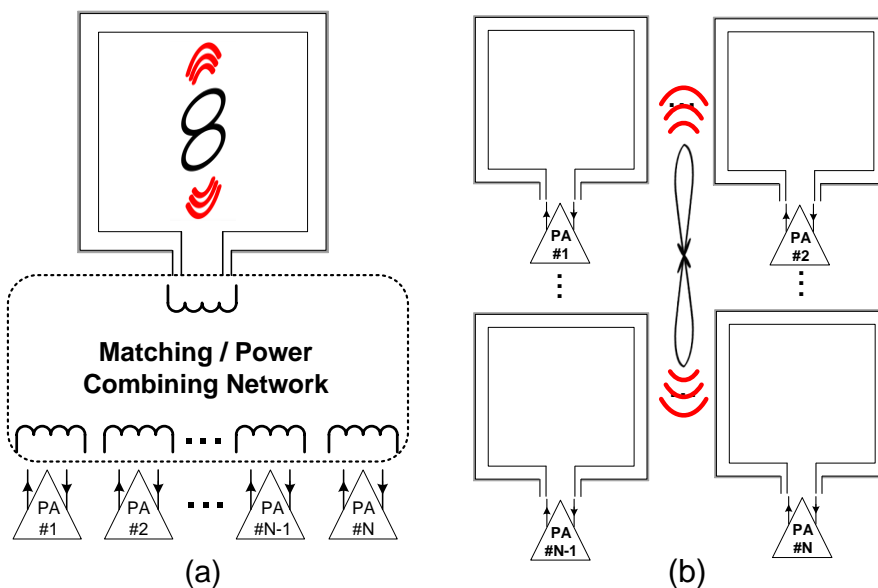


Figure 2-1 (a) Power combining for an SFA using a passive network for impedance matching and power combining. (b) Antenna-array-based spatial power combining with conventional SFAs.

To address these challenges, we propose a multi-feed antenna structure. The multiple feeds are driven simultaneously, and the driving signals are scaled with proper amplitude/phase relationship to actively synthesize the desired RF current/voltage distribution on the antenna. Due to the multi-feed nature, it constructively combines the power from each feed directly on the antenna, eliminating any extra power combining networks and ensuring a high efficiency. Moreover, it is capable of boosting the total radiated power in one single antenna footprint. Furthermore, the multi-feed antenna can be employed in an array to further increase the radiated power.

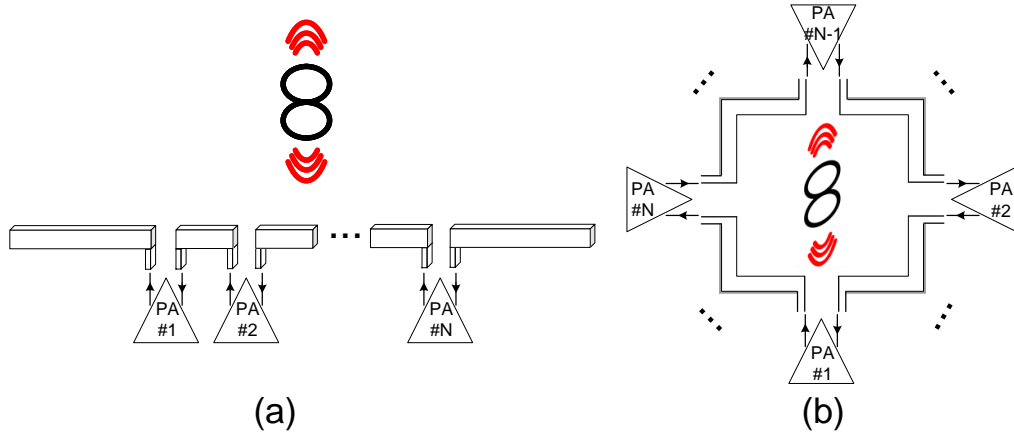


Figure 2-2 (a) Dipole-based MFA for direct on-antenna power combining meanwhile maintaining only one antenna footprint and the same antenna beamwidth. (b) Loop-based MFA that further demonstrates the generality of the MFA structure with enhanced bandwidth for high-speed and complex modulations at mm-Wave.

A multi-feed antenna (MFA) structure is first implemented at X-band [3] [Figure 2-2(a)], which achieves direct on-antenna power combining, showing the potential of simplifying the passive impedance transformation and power-combining network between the wireless transmitter and antenna for high-output power and system power efficiency. Compared with antenna-array-based spatial power-combining technique, it only occupies a single-antenna footprint and maintains a wide single-element beamwidth. Based on the proposed MFA concept, Chi et al. [4] demonstrated a mm-Wave 60-GHz transmitter in a 45-nm CMOS SOI process that employs a multi-feed slot dipole antenna and achieves an

output power of +27.9 dBm/element and EIRP of +33.1 dBm/element, both of which are the best reported values among the state-of-the-art silicon-based 60-GHz transmitters; this demonstration further verifies the advantage of on-antenna power combining. However, the design in [3] shows limited operation bandwidth (4%–5% fractional bandwidth) due to the narrowband nature of the slot dipole antenna.

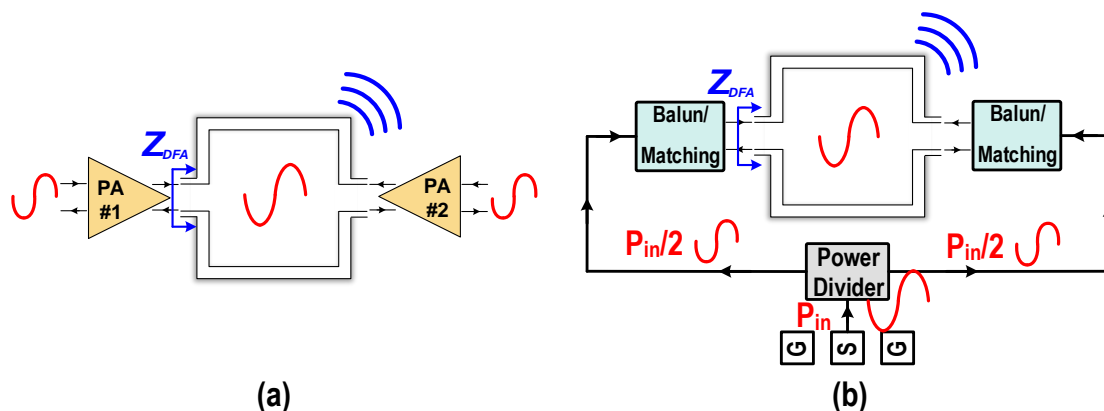


Figure 2-3 (a) DFA driven by two PAs in electronics-antenna integration. (b) DFA testing structure to mimic the scenario in (a).

To facilitate high data-rate 5G communications, a broader bandwidth is preferred. Therefore, a loop-based dual-feed antenna (DFA) structure [Figure 2-2(b)] is further proposed to enhance antenna bandwidth [5]. Moreover, the newly proposed loop-based MFA demonstrates that the MFA concept can be applied to other types of antenna structures for different applications. This work directly proves the generality of the MFA concept. Advances in silicon manufacturing have reduced the cost of mm-Wave electronics and enabled consumer use. A set of frequencies are beginning to emerge as candidates for 5G: 28, 38, and 73 GHz [6]. Because they have lower oxygen absorption rates, making them viable for long-distance communications. They also function well in a multipath environment and thus can be applied for non-line-of-sight communications [7], [8]. The channel properties and potential service outages at these frequencies have already been studied [9], [10]. The existing data and research combined with the spectrum availability

make these three frequencies the starting point for 5G mm-Wave prototyping. The advantage of the proposed DFA over conventional single-feed antenna (SFA) lies in its direct on-antenna power combining capability, especially when the DFA is assembled together with active electronics [Figure 2-3(a)], such as PAs. To facilitate the experiment demonstration, we implement input feeding networks, i.e., power divider, balun, and matching network, for the DFAs [Figure 2-3(b)], which drive the DFAs concurrently and mimic the two PAs driving scenario in Figure 2-3(a). Note that these feeding networks are not necessary in practice, since the proposed DFA can be directly driven by two transmitters/PAs [11], [12]. As proof-of-concept designs, the dual-feed 1λ square-loop antennas are designed and characterized at two potential 5G bands, i.e., 38.5 and 73.5 GHz. Conventional single-feed 1λ square-loop antennas are also implemented as reference designs for performance comparison.

2.2 Multi-Feed Slot Antennas at X-Band

2.2.1 Design and Implementation

Figure 2-4 (a) and (b) show the schematics of both the conventional single-feed and proposed multi-feed slot antennas at the operating frequency f_0 with their voltage distributions. Assuming a narrow slot width, the voltage distribution on the slot can be approximated as

$$V(x) = V_0 \sin \left[k \left(\frac{L}{2} - |x| \right) \right] \text{ and } -\frac{L}{2} \leq x \leq \frac{L}{2} \quad (2-1)$$

where k is the wave number, L is the total length of the slot antenna, and V_0 is the maximum voltage amplitude on the slot. This distribution assumes that the voltage is zero at the edges of the slot ($x = \pm L/2$) [13].

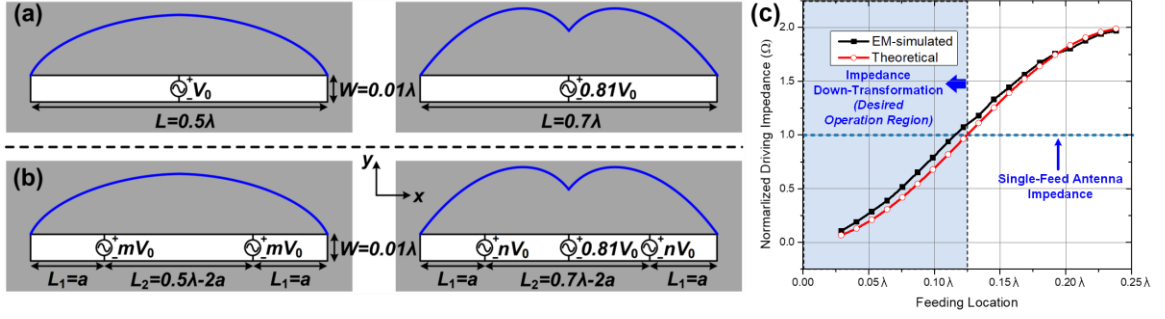


Figure 2-4 (a) A conventional single-feed 0.5λ slot antenna and a 0.7λ slot antenna at f_0 . (b) The proposed multi-feed slot antenna schemes with a two-feed 0.5λ slot antenna and a three-feed 0.7λ shown as examples. (c) Theoretically calculated and EM-simulated driving impedances of the two-feed 0.5λ slot antenna vs. feeding locations.

The multi-feed antenna is excited in the way that the driven voltage signal at each feed matches the voltage distribution of a conventional single-feed slot antenna at the corresponding feed locations. Therefore, the multi-feed antennas in Figure 2-4b will radiate exactly as a conventional single-feed slot antenna at f_0 in Figure 2-4a. In parallel, the driving power from all the feeds are constructively combined on the multi-feed antenna, enabling antenna-level power combining without additional power combining networks. The slot antennas shown in Figure 2-4 are designed on a 20mil-thick Rogers® 3003 substrate. Input feeding networks are designed to distribute the input power from the 50Ω connector to all the antenna feeds only to facilitate the testing. In practice, multiple transmitters can drive all the antenna feeds concurrently, and the input feeding network for power dividing can be eliminated. Note that the proposed multi-feed antenna structure can be applied to not only slot antenna or dipole antenna but also other types of antennas. In this paper, slot antennas are selected for the proof-of-concept demonstration. Assuming that the two-feed 0.5λ slot antenna and the conventional single-feed 0.5λ slot antenna have an identical voltage distribution and the same total radiated power, the driving impedance of the two-feed slot antenna is derived as

$$R_{2feed} = 2R_r \sin^2\left(\frac{2\pi a}{\lambda}\right) \quad (2-2)$$

where R_r is the radiation resistance of the single-feed 0.5λ slot antenna, a is the distance between the feeding location and the edge of the slot shown in Figure 2-4b.

For the two-feed 0.5λ slot antenna, the EM-simulated and calculated driving impedances by equation (2-2) for different feeding locations are plotted in Figure 2-4c. Note that the locations of the multi-feeds can be selected to optimize the driving impedance to facilitate the designs of their transmitters or power amplifiers.

In this two-feed 0.5λ slot antenna design, a feeding location $a=0.125\lambda$ is selected which gives a driving impedance of 860Ω . To synthesize an identical voltage distribution as a single-feed 0.5λ slot antenna, the amplitudes and phases of the two driving voltages should be the same. The 3D EM model of the two-feed 0.5λ slot antenna is displayed in Figure 2-5b. The simulated peak antenna gain is 4.97dBi with a radiation efficiency of 87% at 10.4GHz. A conventional single-feed 0.5λ slot antenna is designed as a reference with a simulated peak antenna gain of 4.57dBi and a radiation efficiency of 89% at 10.6GHz.

The 3D EM model of the three-feed 0.7λ slot antenna with the equivalent circuit model of the matching networks is shown in Figure 2-5c. The voltage distribution on the three-feed slot is engineered to be identical as a single-feed 0.7λ slot antenna. The first feed is placed at the center of the slot, while the locations of the other two feeds are chosen so that the input power at all the three feeds are the same to ease the input feeding network design. The driving impedances of the center feed and the feeds on the side are $677\Omega//210\text{fF}$ and $821\Omega//30\text{fF}$, respectively. The simulated radiation efficiency including the feeding network is 87% with a simulated peak gain of 4.58dBi at 10.3GHz. A conventional single-feed 0.7λ slot antenna is designed as a reference with a simulated peak antenna gain of 5.1dBi and a simulated radiation efficiency of 90% at 10.1GHz.

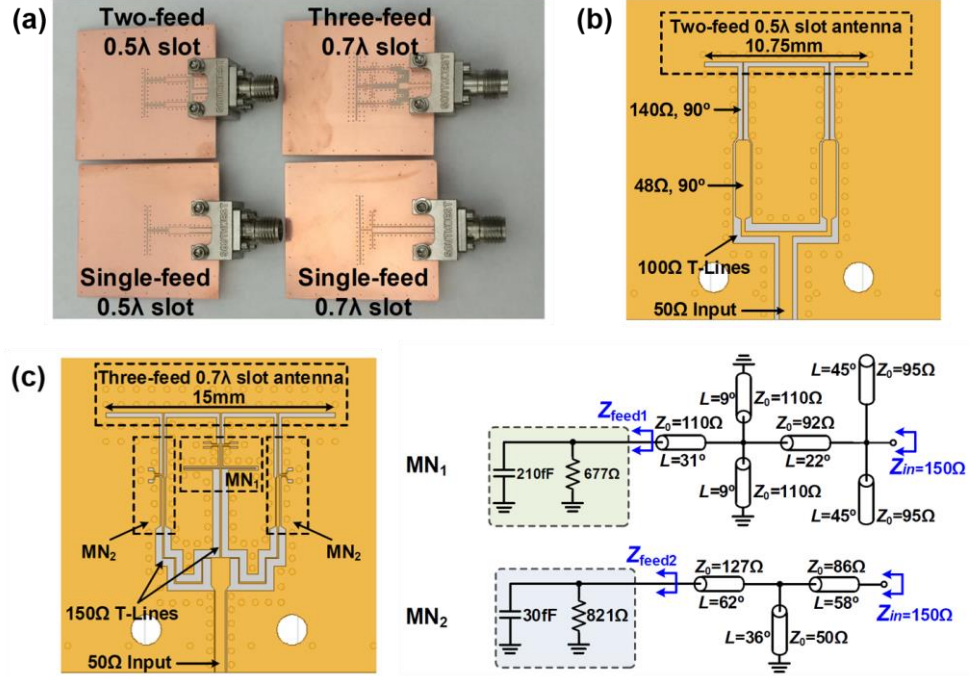


Figure 2-5 (a) Fabricated samples. (b) The 3D EM model of the two-feed 0.5λ slot antenna. (c) The 3D EM model of the three-feed 0.7λ slot antenna with the equivalent circuit model of the matching networks.

2.2.2 Measurement

The fabricated prototypes of the multi-feed and single-feed antennas are shown in Figure 2-5a. The measurement was performed using an R&S VNA (ZVA24) with a separation of 66cm between a standard X-band horn antenna and the antenna under test. The measured return loss and the peak antenna gain versus the operating frequency of the four antenna samples are summarized in Figure 2-6. All the four samples achieve good input matching around their center frequencies. The peak gain for all the samples at their center frequencies are between 4.7 and 5.0dBi, matching well with the 3D EM simulations.

The measured E-plane and H-plane patterns are shown in Figure 2-7 and Figure 2-8. Good agreement between the simulation and measurement results is achieved for both the two-feed 0.5λ slot and the three-feed 0.7λ slot antenna. In addition, the radiation

patterns of the multi-feed antennas closely match with the single-feed reference antennas. This verifies that the multi-feed antennas can actively synthesize the desired voltage/current distribution and thus achieve identical radiation characteristics as conventional single-feed antennas. Moreover, the driving power split by the input feeding network to all the feeds eventually combine on the multi-feed antenna. This unique antenna-level power combining can substantially increase the transmitter total radiated power, EIRP, and DC-to-RF efficiency with a very compact antenna footprint.

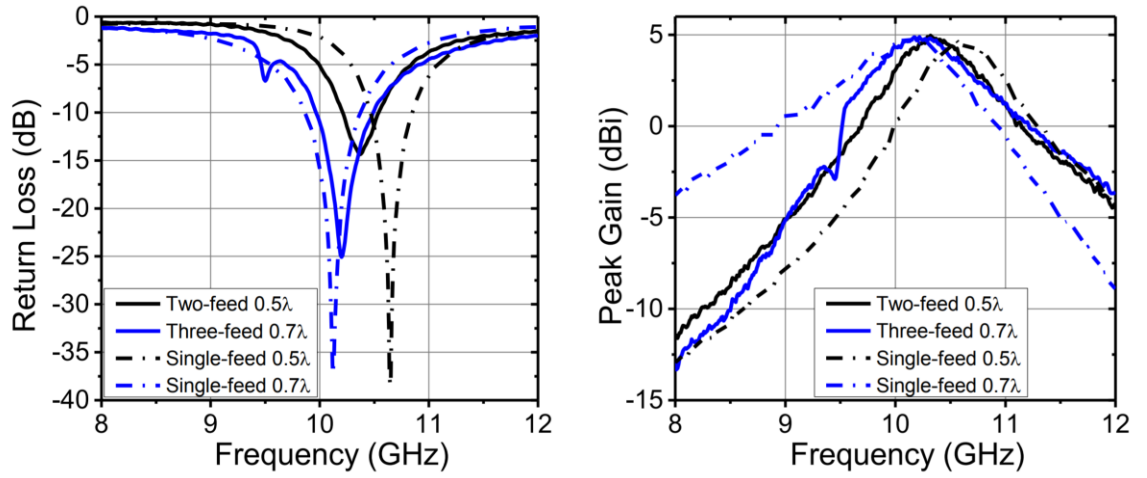


Figure 2-6 Measured return loss and peak antenna gain versus frequency.

2.2.3 Conclusion

A multi-feed antenna structure is proposed to synthesize the desired radiation pattern. Well matched radiation patterns between the multi-feed antennas and the conventional single-feed antennas are achieved in measurements, demonstrating the unique antenna-level power combining capability of the multi-feed antennas.

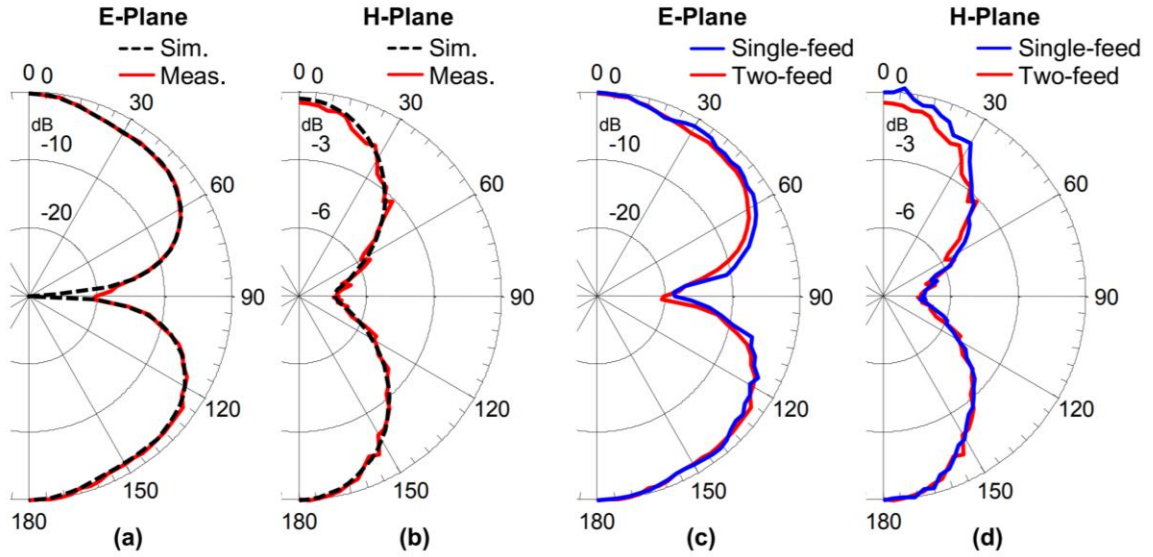


Figure 2-7 (a) (b) Measured and simulated radiation patterns of the two-feed 0.5λ slot at 10.4GHz. (c) (d) Comparisons between the measured radiation patterns of the two-feed and single-feed 0.5λ slot antenna.

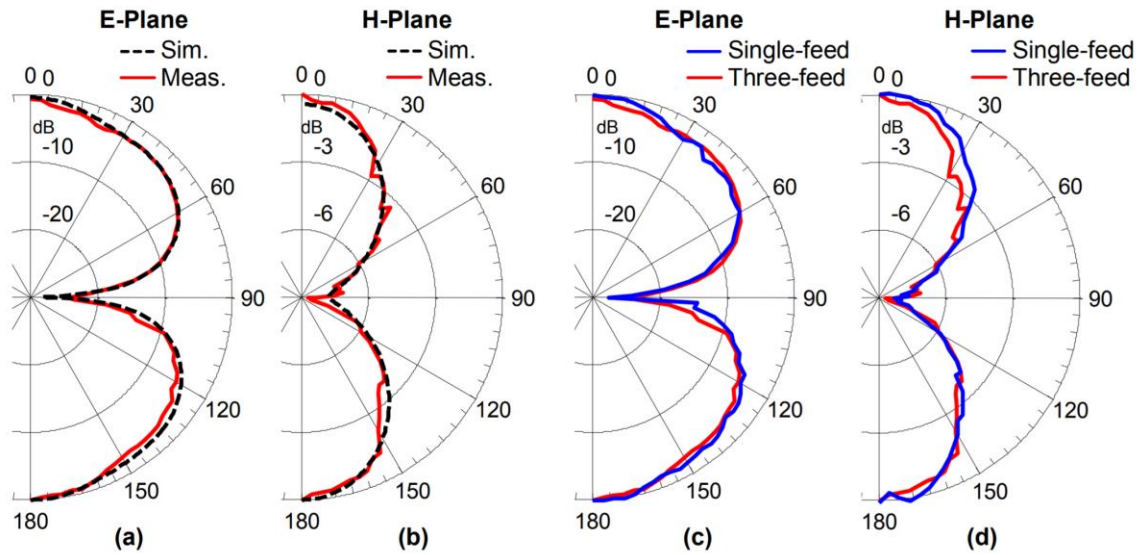


Figure 2-8 (a) (b) Measured and simulated radiation patterns of the three-feed 0.7λ slot at 10.3GHz. (c) (d) Comparisons between the measured radiation patterns of the three-feed and single-feed 0.7λ slot antenna.

2.3 Dual-Feed Square Loop Antennas at Mm-Wave 5G Bands

The current/voltage distribution on the antenna fully determines the radiation characteristics of the antenna itself [13]. In the proposed dual-feed square loop antenna, the amplitude and phase of the driving signals are combined in a way that the same current/voltage distribution is synthesized compared to its conventional single-feed counterpart. Therefore, identical antenna radiation characteristics can be realized with direct on-antenna power combining.

2.3.1 Design and Implementation

2.3.1.1 Antenna Characteristics Synthesis

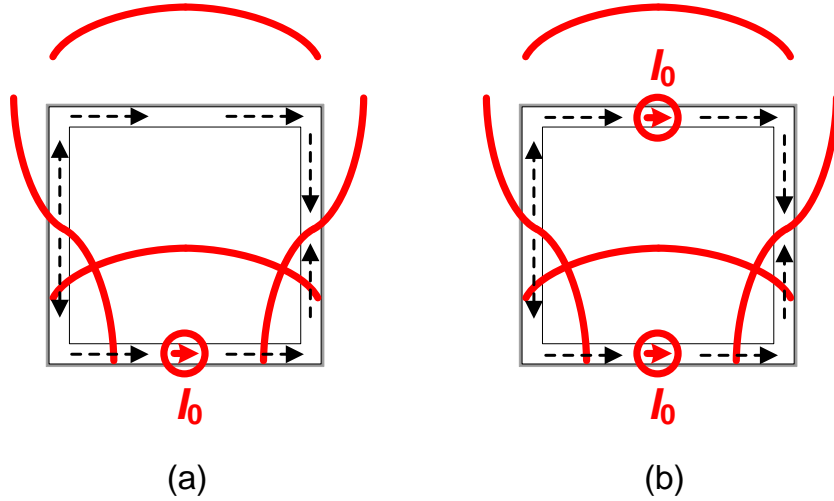


Figure 2-9 (a) Single-feed 1λ square loop antenna with its current distribution at f_0 as the reference design. (b) The dual-feed 1λ square loop antenna with its current distribution at f_0 .

As shown in Figure 2-9(a), for a 1λ square loop antenna, its current distribution is assumed to be sinusoidal for analysis [14]. A standing-wave pattern is formed with the current maximum located at the feed location and the center of the opposite side. Two current nulls locate at the center of the other two perpendicular sides. The amplitude of the maximum current is assumed to be I_0 .

Figure 2-9(b) shows the proposed dual-feed square loop antenna. A second feed is added to the other current maximum location of the loop with the same current excitation I_0 . Identical current distribution is achieved in the dual-feed case because of symmetry, which leads to the same radiation patterns of the two antennas. Direct on-antenna power combining is thus achieved without extra passive power-combining network.

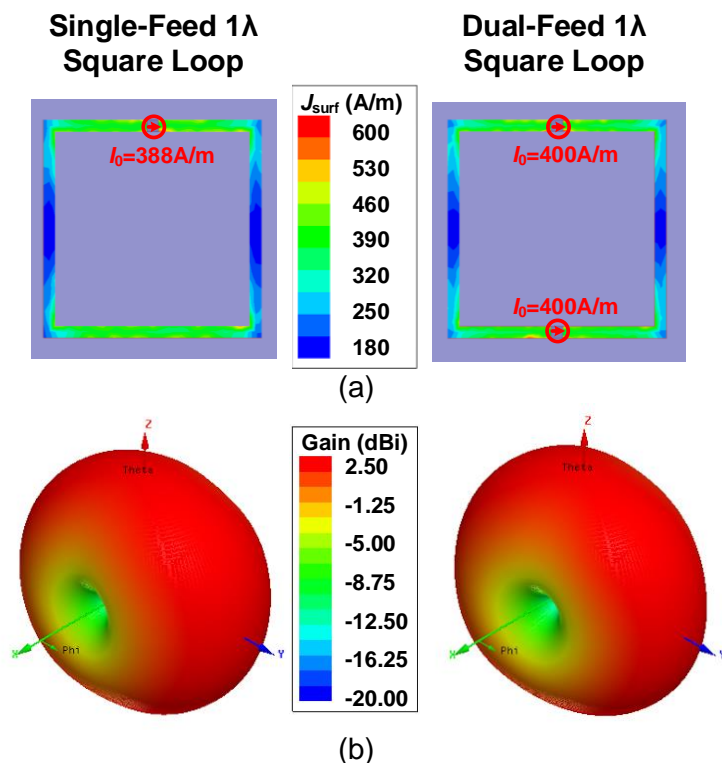


Figure 2-10 EM-simulated (a) surface current distributions and (b) 3-D radiation patterns of the single-feed and dual-feed 1λ square loop antennas at 38.5 GHz.

The proposed DFA is verified using 3-D electromagnetic (EM) simulations. The single-feed and dual-feed 1λ square-loop antennas are designed on a 10-mil-thick RO3003 substrate at 38.5 GHz. The total loop length is 8 mm. In order to facilitate the comparison, matching or feeding network is excluded in this verification step to eliminate its influence. The 3-D EM-simulated surface current distributions and the far-field radiation patterns of the two antennas are shown in Figure 2-10. A close match is achieved in the 3-D EM simulations, verifying that the proposed DFA indeed synthesizes the identical current

distribution and radiation pattern as its single-feed counterpart. The small difference in the maximum current values is due to the finite length of the feeds as well as a slight frequency shift shown in Figure 2-12. Nearly 100% simulated radiation efficiency is achieved in both cases, ensuring that the power from the two feeds are efficiently combined directly on the antenna. A closer comparison of the E- and H-planes is also summarized in Figure 2-11(a) and (b), which further proves the synthesis of the same current distribution as the SFA.

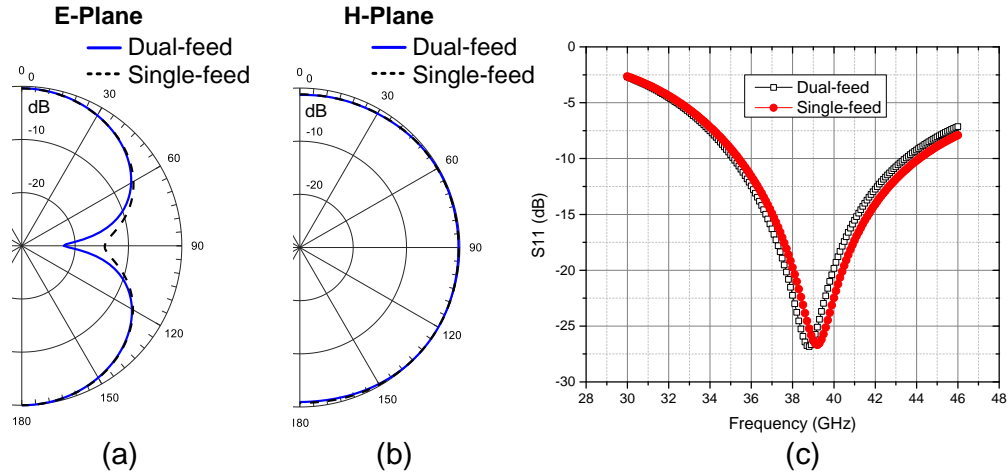


Figure 2-11 Comparison in the (a) E-plane, (b) H-plane, and (c) S_{11} bandwidth between dual-feed and single-feed 1λ square loop antennas.

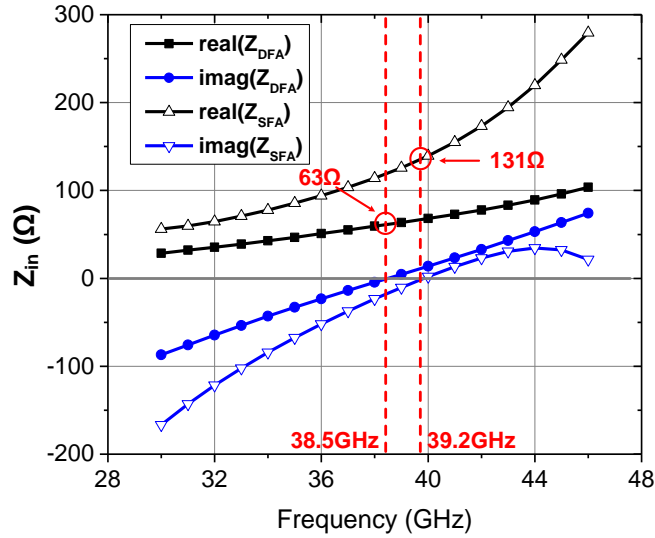


Figure 2-12 Simulated input impedance of the single-feed and dual-feed 1λ square loop antennas versus frequency.

2.3.1.2 Impedance Down-Scaling

The antennas are designed to operate at its first resonance point, so the input impedance of the antennas at f_0 is purely real. The input matching bandwidth ($S_{11} < -10$ dB) of the antennas is calculated and plotted in Figure 2-11(c). The DFA maintains the same bandwidth compared to the conventional SFA, proving that not only radiation characteristics but also antenna bandwidth is preserved in the dual-feed configuration. A well-matched inherent 20% fractional bandwidth is achieved for the antenna structure, showing the potential of the proposed DFA to support high data-rate communications. Inherent impedance down-scaling is also achieved in the proposed DFA structure. With the identical current distribution on the loop antennas, the SFA and DFA radiate out the same power, as

$$\frac{I_0^2 R_{SFA}}{2} = 2 \frac{I_0^2 R_{DFA}}{2}, \quad (2-3)$$

where R_{SFA} is the driving resistance of the single-feed square loop antenna, and R_{DFA} is the input impedance of each feed in the dual-feed square loop antenna. Equation (2-3) can be further simplified as

$$R_{DFA} = R_{SFA}/2. \quad (2-4)$$

The driving impedance of the dual-feed square loop antenna (R_{DFA}) becomes half of that of the single-feed square loop antenna (R_{SFA}). This inherent impedance down-transformation by a factor of 2 is particularly beneficial for the antenna to interface with high-power and high-efficiency PAs. The 3-D EM-simulated R_{SFA} and R_{DFA} versus frequency are plotted in Figure 2-12. The single-feed square loop antenna resonates at 39.2 GHz with an input resistance of 131 Ω , while the dual-feed square loop antenna resonates

at 38.5 GHz with a driving impedance of $63\ \Omega$, verifying the impedance down-transformation by a factor of 2 by the DFA. The DFA concept can be further extended to a greater number of feeds to achieve MFAs, as presented in the authors' recent work [3], [4]. The main purpose of this study is to present the generality of the on-antenna power combining as well as providing a more broadband antenna solution to the upcoming 5G communications.

2.3.1.3 Application Example

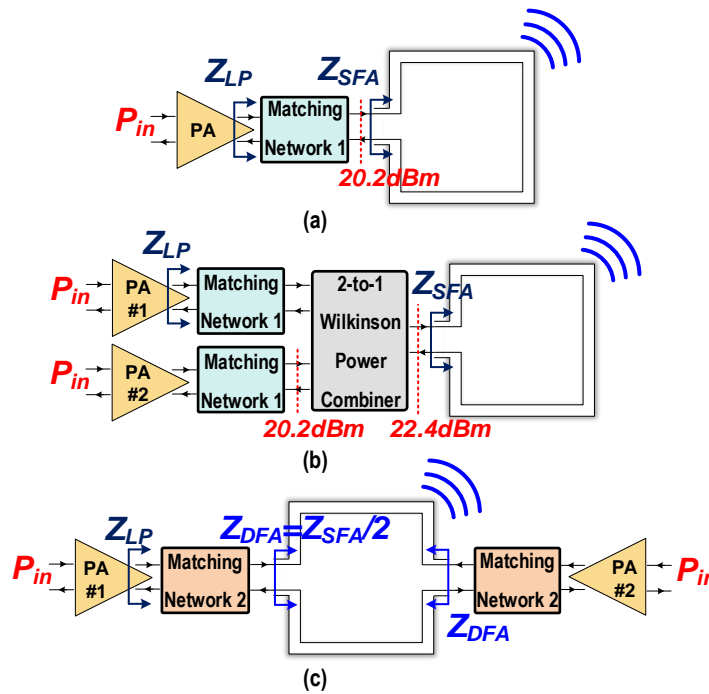


Figure 2-13 Application example (a) one single PA drives the conventional SFA. (b) Two PAs are combined by the two-way Wilkinson power combiner and drive the SFA. (c) Two PAs drive the proposed DFA.

An application example is presented here to further explain the advantage of the direct on-antenna power combining of the proposed DFA. The PA used in the following discussion has 20.2-dBm output power (when driving a matched $50\text{-}\Omega$ load) at around 40 GHz [15]. In the first case, one single PA is used to drive a conventional SFA, as shown in Figure 2-13(a). The SFA input impedance Z_{SFA} is transformed to the load-pull impedance

of the PA (Z_{LP}) by its on-chip matching network (MN_1) with a passive loss of L_I . In the second case [Figure 2-13(b)], two PA outputs are combined by an on-chip Wilkinson power combiner and then fed to the SFA. Typical insertion loss of an on-chip Wilkinson power combiner is 0.8 dB [15]. Thus, a total output power of 22.4 dBm is achieved in this scenario. Figure 2-13(c) shows the third case where the two PAs drive the proposed DFA directly with matching network MN_2 . Due to the direct on-antenna power combining of the DFA [Figure 2-13(c)], the 0.8-dB loss from the on-chip Wilkinson combiner in scenario 2 is eliminated. This directly improves the system power efficiency by a factor of 1.2 \times . Moreover, DFA also achieves inherent impedance down-scaling ($Z_{DFA} = 0.5 \times Z_{SFA}$), the loss L_2 of its matching network (MN_2) is expected to be smaller than that (L_I) in case 1 and 2 (MN_1) [16]. This further enhances the total system efficiency. If we compare the case 3 with case 1, the DFA doubles the total radiated power while achieving similar or better power efficiency. If we compare the case 3 with case 2, the DFA achieves similar output power while ensuring better power efficiency.

This application example clarifies the advantage of direct on-antenna power combining by the DFA. Moreover, in two of the authors' recent publications [3], [4], the antennas are driven in a multi-feed fashion, which makes it possible to achieve high-transmitter output power; the output power of the 60-GHz design in [4] outperforms the state-of-the-art designs by at least 4dB.

2.3.1.4 Feeding Network

The antenna feeding network is only designed to facilitate the antenna testing. In practice, these feeding networks are not necessary, since the proposed MFA can be directly driven by multiple transmitters/PAs. The EM model of the dual-feed square loop antenna together with its feeding network is shown in Figure 2-14. The driving signals at the two feeds have the same amplitudes and phases due to symmetry. A $\lambda/4$ clearance around the

loop antenna in the ground plane is created to minimize reflection from the ground plane. Z_{in1} is the input impedance of the DFA. A $\lambda/4$ differential transmission line (T-line) with characteristic impedance of Z_{o1} converts Z_{in1} into Z_{in2} ($Z_{in2} = Z_{o1}^2/Z_{in1}$). Then, another $\lambda/4$ T-line transforms the single-ended impedance $Z_{in2}/2$ to $2Z_{in3}$ ($2Z_{in3} = Z_{o2}^2/0.5Z_{in2}$). Meanwhile, the balun converts the differential excitation into in-phase signals. The routing line with a length of $N \times \lambda/2 + \lambda/4$ performs another impedance transformation ($2Z_{in4} = Z_{o3}^2/Z_{in3}$). Finally, Z_{in4} is matched to 50Ω by the $\lambda/4$ T-line of Z_{o4} . There is no specific requirement for the Z_{in1} , Z_{in2} , and Z_{in3} values. Here, Z_{o1} , Z_{o2} , and Z_{o3} are chosen to achieve good input matching and bandwidth, within the achievable Z_o range limited by the PCB fabrication. Similar matching technique is applied to implement the feeding network of the SFA for comparison purpose.

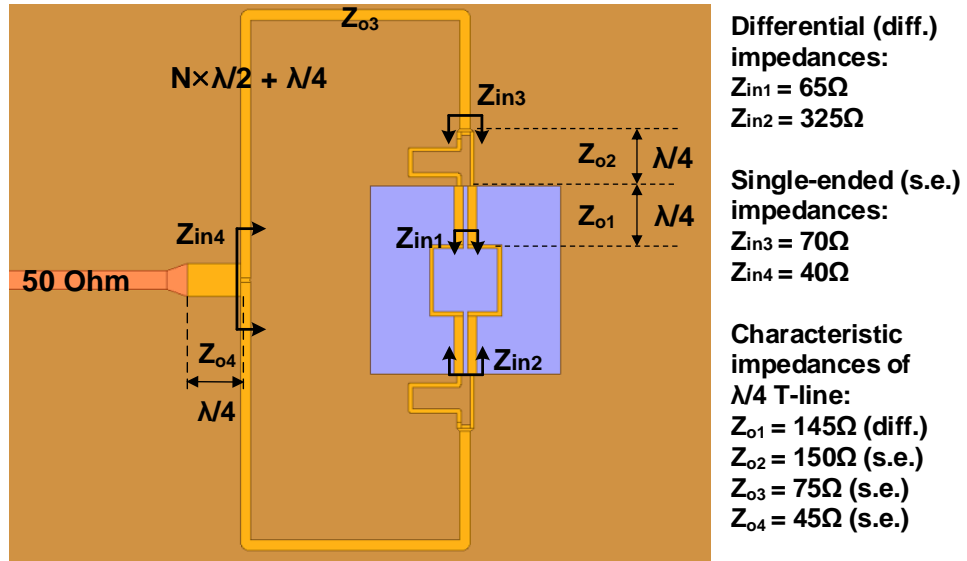


Figure 2-14 Feeding network of the proposed DFA.

2.3.1.5 Effect of Finite Ground Plane

When the ground plane is finite, the edge diffractions become radiation sources [17]. A ground dimension of $30\text{ mm} \times 30\text{ mm}$ is first chosen for mechanical stability consideration. However, finite ground effect manifests itself in a way that the antenna

patterns get distorted. Such behaviors become more significant at mm-Wave frequencies. Thus, the antenna ground size is optimized for smooth radiation patterns. The original and final antenna ground dimensions and their corresponding radiation patterns are summarized in Figure 2-15. When the ground plane is larger, the patterns start to undulate, because of the contribution from a larger electrical spacing of the diffraction sources (ground edges). The final ground size is optimized to be 23 mm \times 15 mm, with the corresponding radiation patterns being much smoother compared to those with the original ground size. The antenna beamwidth is also restored with the shrunken ground dimensions. Therefore, due attention should be given to the ground effect on the antenna radiation patterns, especially at mm-Wave frequencies.

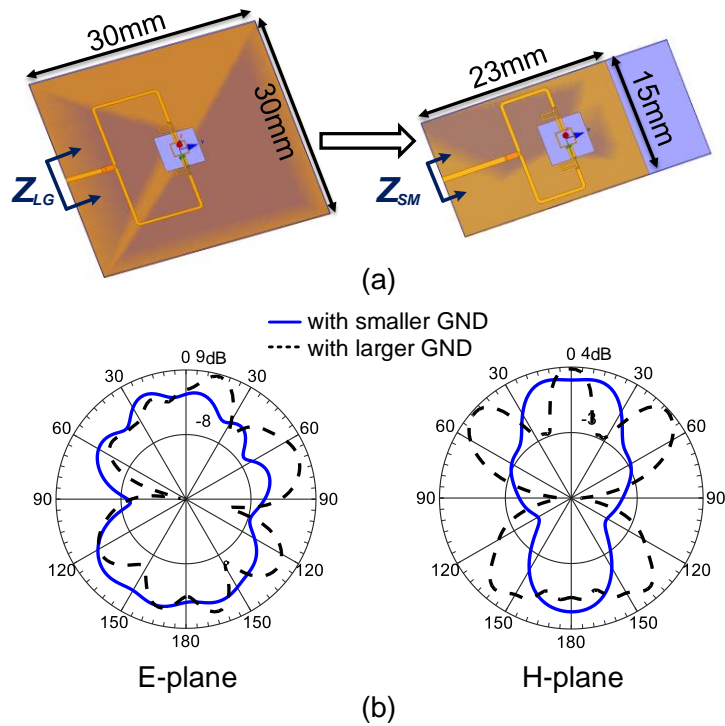


Figure 2-15 (a) DFA with different ground geometries. (b) Radiation pattern comparison between the DFA with a large ground size and small ground size.

The ground effect on the antenna input impedance is also simulated. Both real and imaginary parts of the antenna input impedance are plotted in Figure 2-16. Z_{LG} is the

driving impedance of the DFA with the large ground plane as shown in Figure 2-15(a), and Z_{SM} is the input impedance of the same antenna configuration with the small ground plane as shown in Figure 2-15(a). Unlike the obvious ground effect on the radiation patterns, the input impedance remains relatively stable with the change in the ground size, showing the tolerance of the input matching bandwidth to the ground dimensions.

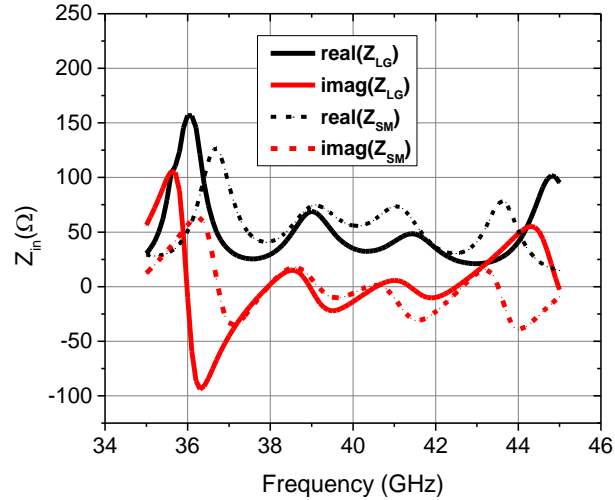


Figure 2-16 Input impedance of the DFA with a large and small ground plane.

2.3.1.6 Full Structure EM Simulation Results for the 38.5-GHz DFA Design

The 3-D EM models of the SFA and DFA are shown in Figure 2-17, together with their corresponding 3-D radiation patterns. For the proposed DFA, the simulated broadside antenna gain is 2.54 dBi with a simulated radiation efficiency of 90% at 38.5 GHz. A conventional SFA is designed as a reference [Figure 2-17(a)] with a simulated broadside antenna gain of 2.40 dBi and a simulated radiation efficiency of 92%. In these 3-D EM simulations, closely matched patterns and radiation efficiency are achieved for the proposed DFA and conventional SFA. The slight difference is attributed to the matching networks.

With ground size optimization, both E- and H-planes achieve smooth patterns, maintaining the original antenna beamwidth. The simulated antenna bandwidth is from 36.8 to 41.4 GHz (12%). The bandwidth reduction compared to the inherent antenna bandwidth is due to the matching network. Because the fabrication-restricted achievable T-line characteristic impedance Z_o on the PCB limits a more broadband matching network implementation. Practically, the matching/feeding network is not necessary or can be much simplified, since the proposed DFA can be directly driven by two transmitters/PAs, and therefore, the inherent antenna bandwidth could be preserved.

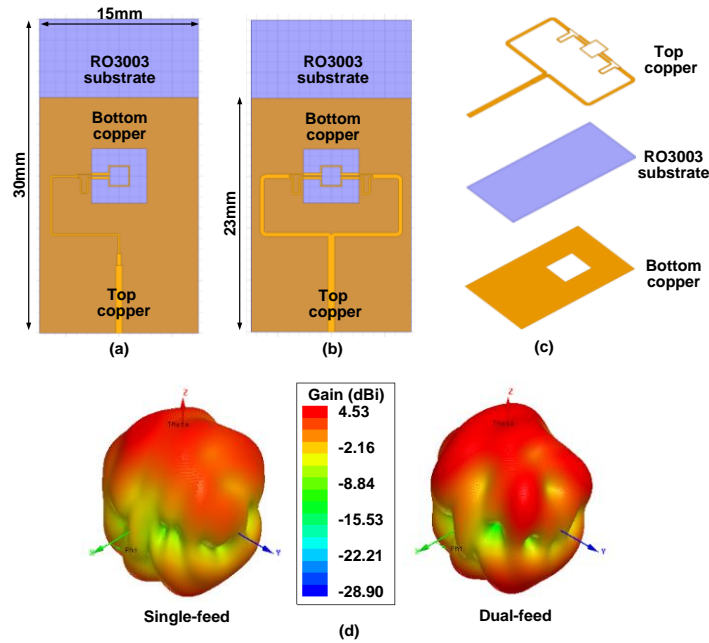


Figure 2-17 The 3-D EM models of the (a) conventional SFA and (b) proposed DFA. (c) Layer stack-up and material used. (d) 3-D radiation patterns of the two antennas.

2.3.1.7 Design Tradeoffs at 73.5GHz

When the operation frequency exceeds 70 GHz, the radiation from the matching/feeding network becomes notable, and therefore, the antenna radiation pattern gets distorted. The reason is that at such high frequencies, the substrate thickness is electrically large enough so that the signal current and ground return current cannot cancel

out at far field. A thinner substrate is helpful to prevent radiation from feeding networks. However, a thinner substrate results in a larger parasitic capacitance between the signal and ground path, which limits the available T-line characteristic impedance (Z_0) range. Taking microstrip line as an example, the fabrication limitation determines the minimum trace width that is achievable, in other words, the maximum Z_0 . With thinner substrate, the maximum impedance of the T-line decreases, which limits the total S_{11} bandwidth after the matching network is integrated. Therefore, a compromise needs to be made for acceptable radiation pattern and bandwidth at the same time.

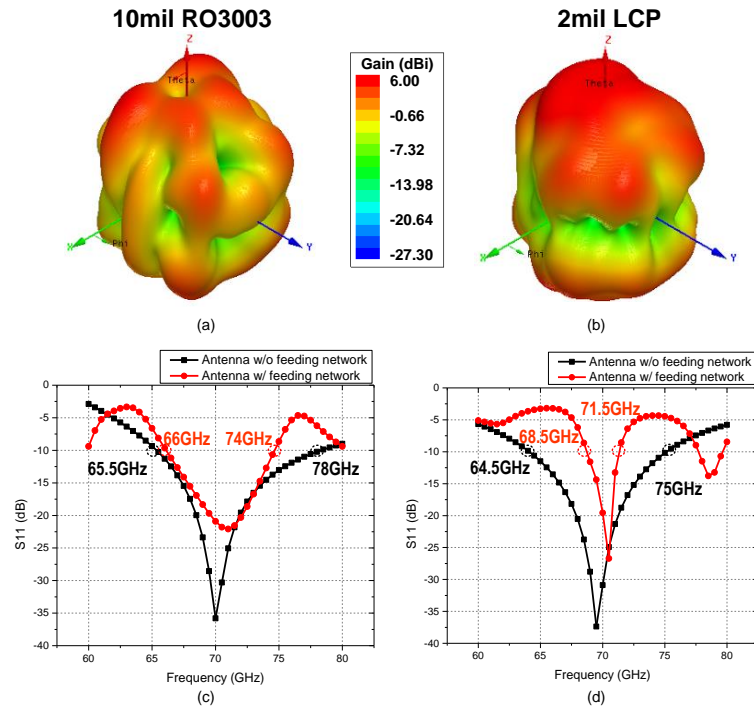


Figure 2-18 3-D radiation pattern of the DFA at 73.5 GHz using (a) 10-mil RO3003 and (b) 2-mil LCP. The simulated S_{11} of the DFA at 73.5 GHz using (c) 10-mil RO3003 and (d) 2-mil LCP.

The 10-mil-thick RO3003 and 2-mil-thick liquid crystal polymer (LCP) are first chosen to implement the 73.5-GHz design and compared in performance. The two types of material have similar electrical properties at mm-Wave frequencies [18]–[21]. The antenna structure [Figure 2-17(b)] is scaled to operate at 73.5 GHz. The simulated antenna pattern

and bandwidth are shown in Figure 2-18. As expected, the antenna radiation pattern using thicker substrate experiences more undulation, while the bandwidth after matching is much wider than that of the same antenna configuration using thinner substrate. Therefore, a compromise (5-mil RO3003) is finally selected as the substrate for the implementation at 73.5 GHz.

The comparisons in E- and H-plane patterns and input matching between the designs on the substrates of three different thicknesses are summarized in Figure 2-19. The design on the 5-mil-thick substrate shows less rippled radiation pattern but maintains a similar bandwidth, compared with the design on 10-mil-thick substrate. It shows that the 5-mil RO3003 can be a good candidate for antenna design around 70 GHz. It is also worth noting that by IC-to-package integration, PAs can directly feed the antenna without feeding network. So thin substrate, such as 2-mil LCP, is preferred.

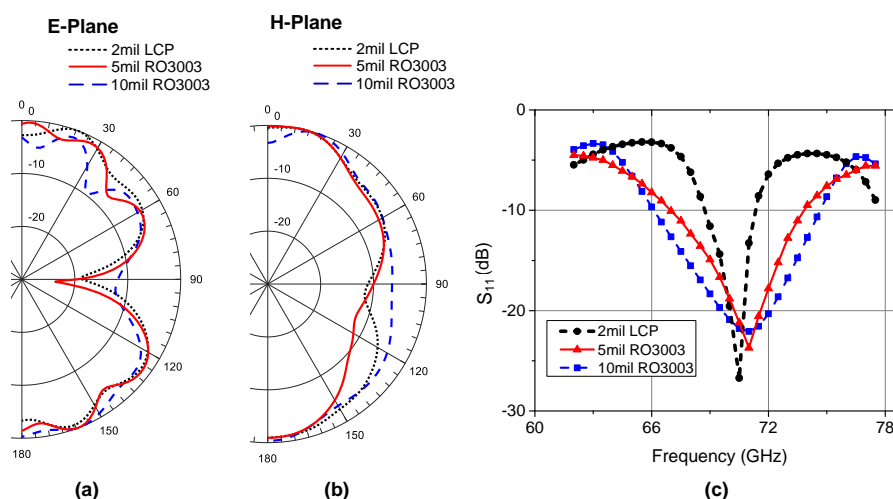


Figure 2-19 Simulated (a) E-plane pattern, (b) H-plane pattern, and (c) S_{11} of the DFA on the substrates of three different thicknesses.

2.3.2 Continuous Wave Measurement Results

To experimentally verify the proposed DFA concept for on-antenna power-combining, dual-feed 1λ square-loop antennas at both 38.5 and 73.5 GHz are fabricated

and measured. Single-feed 1λ square loop antennas are also implemented as reference designs. The photographs of the fabricated antenna prototypes are shown in Figure 2-20.

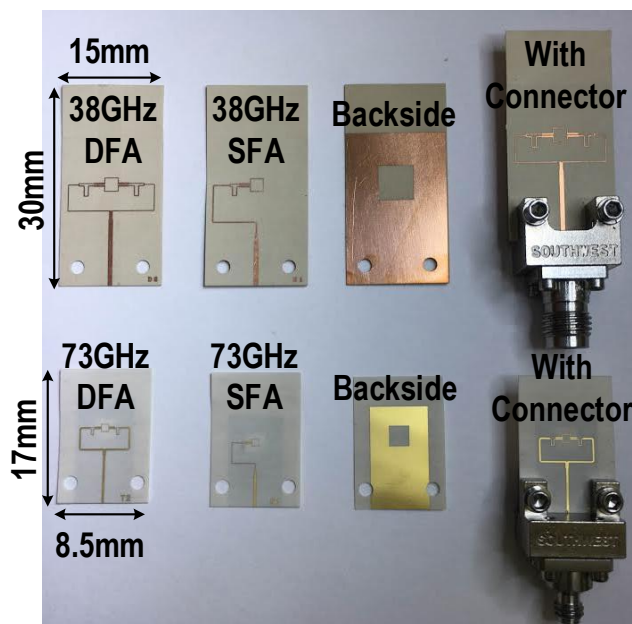


Figure 2-20 Photographs of the fabricated antenna samples using RO3003 substrates. The 38-GHz antennas use 10-mil-thick substrate and the 73-GHz antennas use 5-mil-thick substrate.

The S_{11} of the antennas at 38.5 GHz is directly measured using Agilent E8361C PNA Network Analyzer. Anritsu 37397D Vector Network Analyzer is used to measure the S_{11} at 73.5 GHz, with Anritsu 3742A-EW transmission reflection modules and Anritsu 3738A broadband test set extending the measurement frequency up to 110 GHz. The 38.5-GHz antenna gain and pattern measurement are performed using a signal generator to provide transmitting signal and a power sensor to measure the received signal, with a distance of 83 cm between a standard horn antenna and the antenna under test to ensure far-field characterizations, as shown in Figure 2-21(a). The antenna gain and pattern measurement setup for 73.5 GHz is shown in Figure 2-21(b). The output signal from the signal generator is multiplied by the Virginia Diodes Incorporation V-band source to provide the transmitting signal at 73.5 GHz. On the receiver side, the RF signal is down-

converted to 5 GHz and measured by a spectrum analyzer. An OML V-band source is used to provide local oscillator (LO) signal for the down-conversion mixer. The distance is adjusted to 70 cm for far-field measurement at 73.5 GHz.

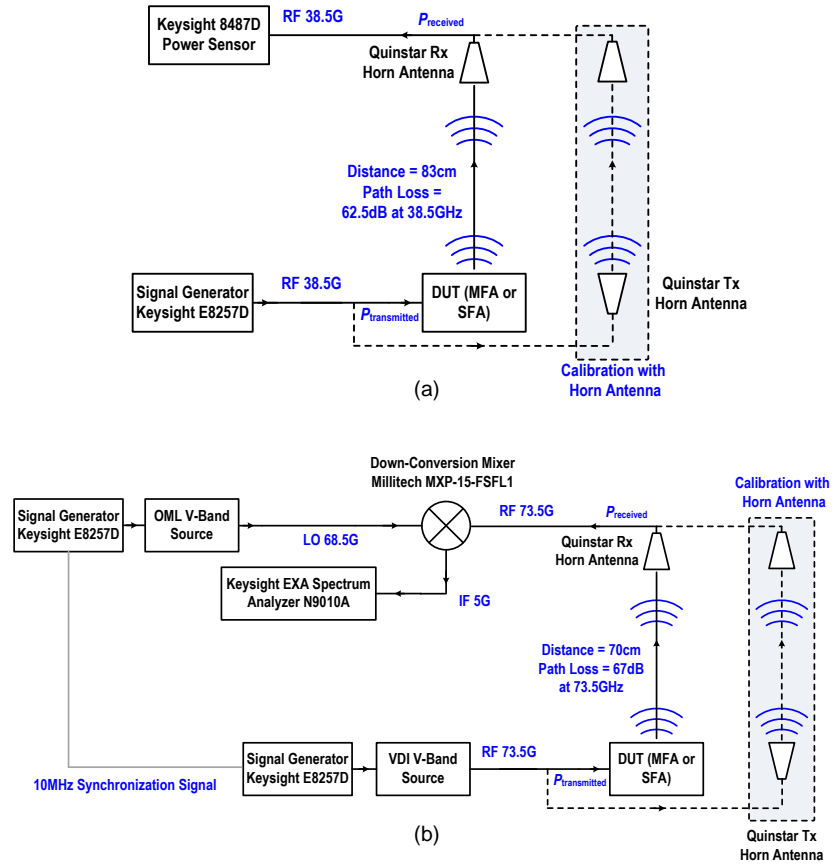


Figure 2-21 Antenna gain and pattern measurement setup for (a) 38.5-GHz antennas and (b) 73.5-GHz antennas.

2.3.2.1 Input Matching and Broadside Antenna Gain

The measured S_{11} versus the operating frequency of the antennas are summarized in Figure 2-22. Excellent agreement in bandwidth is achieved in measurement of the dual-feed and single-feed square loop antennas at 38.5 GHz. The dual-feed 1λ square loop antenna achieves its input matching bandwidth ($S_{11} < -10$ dB) from 36.3 to 40.9 GHz (12%), while its conventional single-feed counterpart shows the same measured bandwidth

[Figure 2-22 (a)]. As shown in Figure 2-22 (b), the 73.5 GHz dual-feed square loop antenna achieves its input matching bandwidth from 67.5 to 78.1 GHz (14.4%), and the single-feed reference design has the input matching bandwidth from 68.5 to 79.5 GHz (15%), still showing well-matched bandwidth for the dual-feed and single-feed square loop antennas.

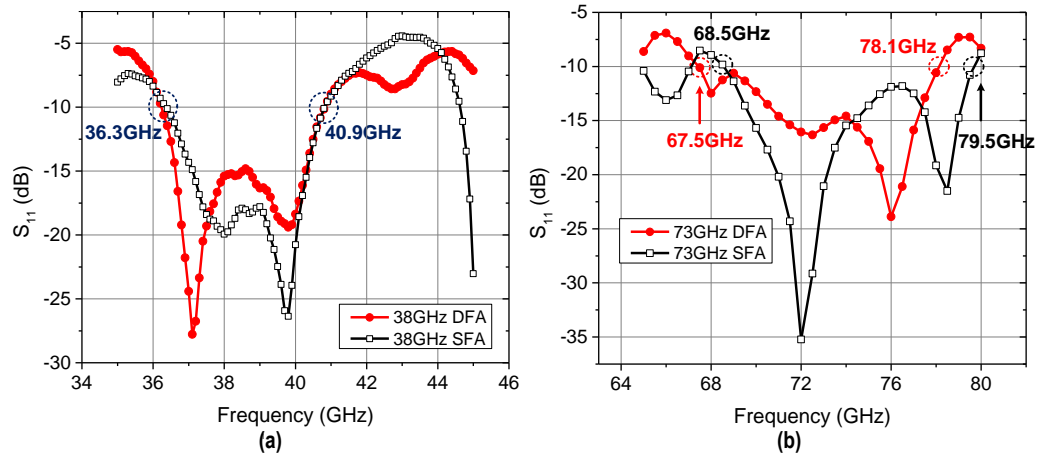


Figure 2-22 Measured S_{11} for the dual-feed and single-feed 1λ square loop antennas (a) at 38.5 GHz and (b) at 73.5 GHz.

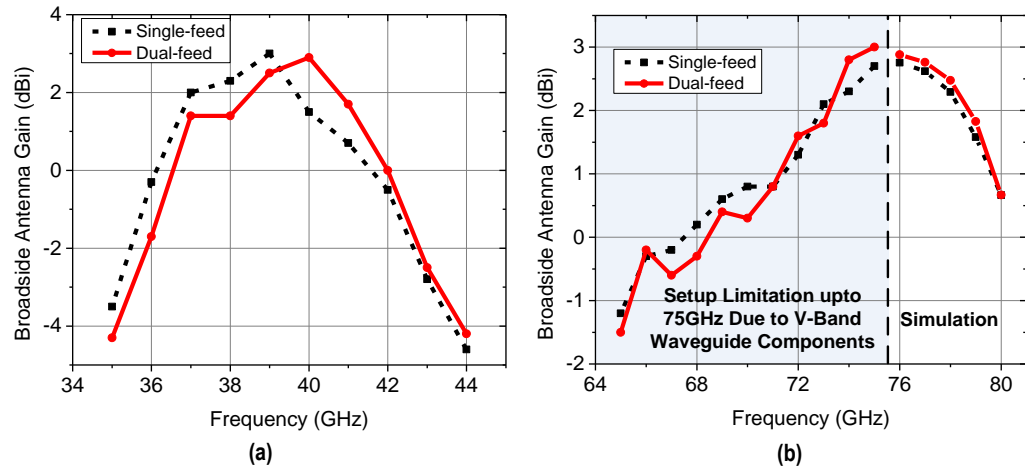


Figure 2-23 Measured broadside antenna gains for the dual-feed and single-feed 1λ square loop antennas (a) at 38.5 GHz and (b) at 73.5 GHz.

Compared with the authors' recent work [3], the bandwidth of the proposed DFA is substantially improved to support high-speed and complex modulation schemes,

particularly beneficial for 5G communications. If two PAs are used to directly drive the DFA, the input feeding network can be simplified or even eliminated, which can further increase the input matching bandwidth.

The good matching achieved in the measurement directly proves the impedance down-scaling of the DFA compared to the SFA, since the matching networks are designed accordingly based on the input impedances Z_{DFA} and Z_{SFA} . With this inherent impedance down-scaling of the DFA, the required impedance-transformation ratio is lowered, resulting in simplified PA output network with improved passive loss and bandwidth.

Figure 2-23 summarizes the measured broadside antenna gains versus the operating frequency, showing well-matched antenna gain performance of the SFA and DFA across all the frequencies. The same amount of input power $P_{transmitted}$ is fed to the device under test (DUT) (DFA or SFA), and the corresponding received power $P_{received}$ is measured. Almost identical received power level is captured in the two cases. This experimentally proves that half $P_{transmitted}$ is distributed to each DFA feed, and the input power to the two feeds is indeed combined on the antenna and then constructively radiated out. The antenna gain (G_{DUT}) is calculated using $G_{DUT} = P_{received} - P_{transmitted} + L_{path} - G_{horn}$, where L_{path} is the path loss in free space, and G_{horn} is the gain of the standard horn antenna. Thus, the same received power results in the same antenna gain. The measured broadside antenna gains of the DFA are 2.9 and 3 dBi, at 38.5 and 73.5 GHz, respectively. They closely match the measured values of the SFA samples, demonstrating the on-antenna power combining.

2.3.2.2 Absolute Radiated Power to Demonstrate On-Antenna Power Combining

The measured absolute radiated output power at 38.5 GHz in both E- and H-planes is summarized in Figure 2-24. If the driving power per antenna feed is identical, the total radiated power or EIRP of a DFA is twice of the EIRP of an SFA.

In this measurement, the power delivered into each antenna feed (one feed for SFA and two feeds for DFA) is made equal (8.5 dBm/feed) to mimic the scenario where the SFA and DFA are, respectively, driven by one or two identical PAs. As shown in Figure 2-24, the output power of the DFA well matches with that of the SFA +3 dB case. Thus, these measurement results directly prove the on-antenna power combining of the proposed DFA, since equal power is fed into each feed of the DFA and twice amount of output power is indeed captured in the measurement. Moreover, it further verifies the advantage of the proposed DFA to achieve higher output power.

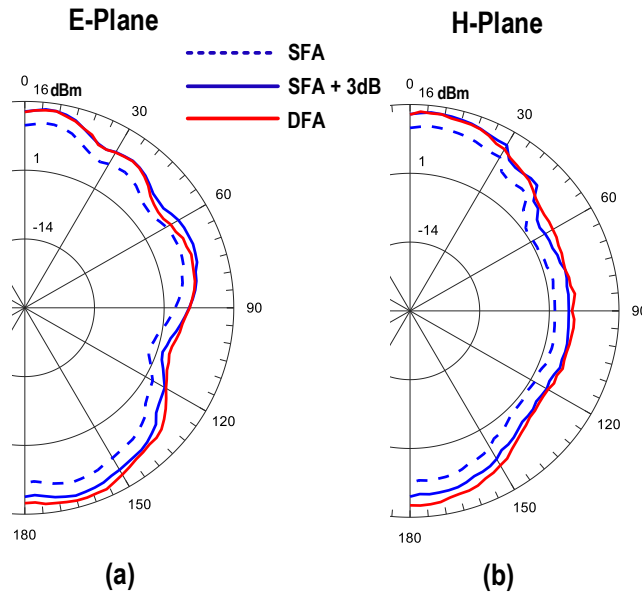


Figure 2-24 Measured absolute output power of both SFA and DFA in (a) E-plane and (b) H-plane.

2.3.2.3 Antenna Radiation Patterns

The measured 38.5- and 73.5-GHz far-field radiation patterns of the 1λ square loop antennas are summarized in Figure 2-25(a) and (b), respectively. The comparisons between the proposed DFA and the conventional SFA are also shown in Figure 2-25(c). Good agreements between the simulation and measurement results are achieved for both designs. More importantly, the measured and simulated radiation patterns of the DFA closely match

with those of the reference SFA, which verifies that the DFA actively synthesizes the desired current distribution on the antenna and thus achieves identical radiation patterns as the conventional SFA.

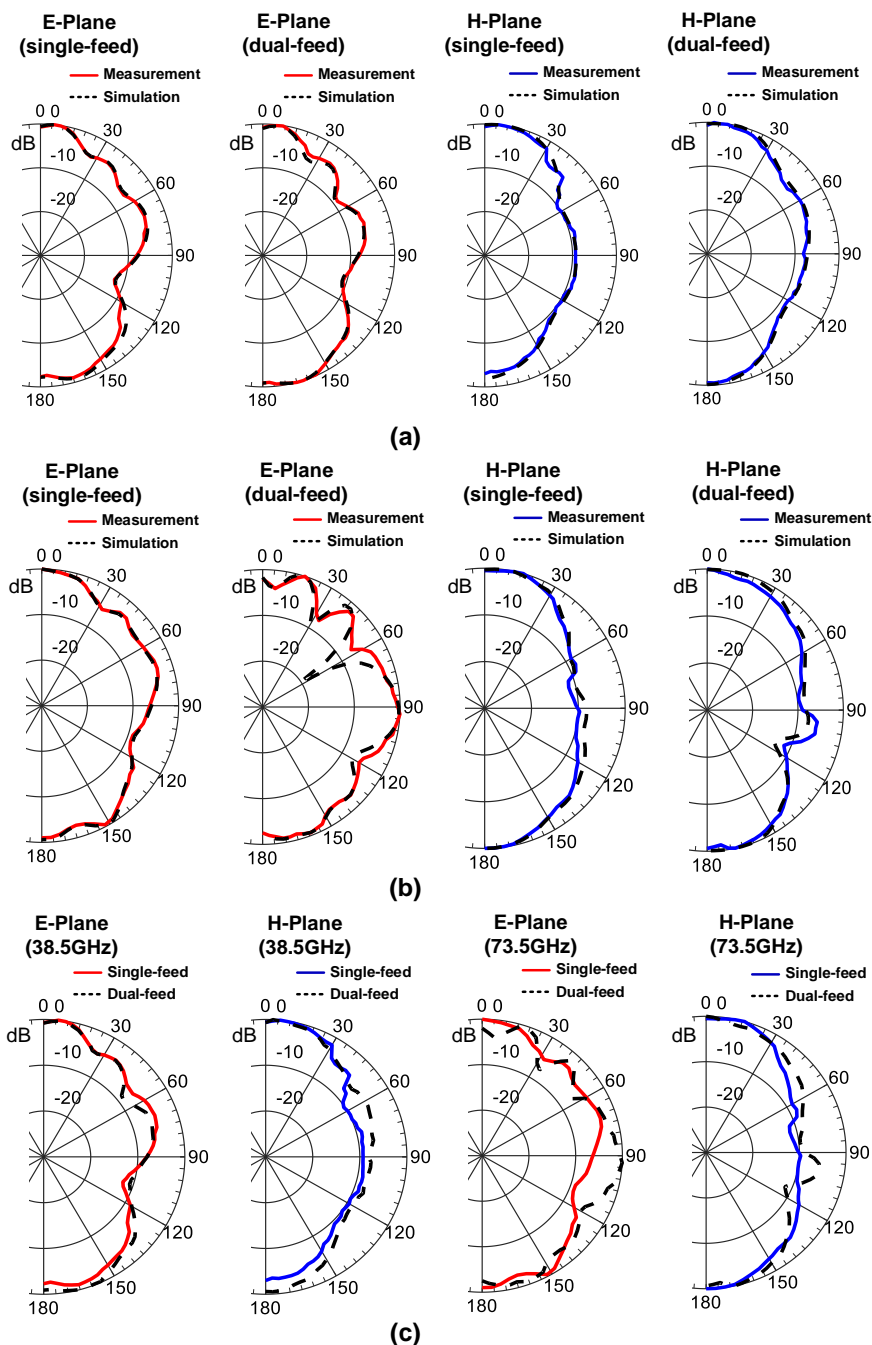


Figure 2-25 Measured and simulated radiation patterns of the DFA and SFA (a) at 38.5 GHz and (b) at 73.5 GHz. (c) Comparison between the DFA and SFA at both 38.5 and 73.5 GHz.

Moreover, together with the agreement in the broadside antenna gain measurement results in Figure 2-23, the DFA has the same absolute antenna gain as the SFA. This further verifies the on-antenna power combining of the proposed DFA, since in this experimental setup, the total input power is first split by the input power divider, distributed to the two different antenna feeds, and eventually combined directly on the DFA structure for radiation. Due to the achieved direct on-antenna power combining, lossy power combiner can be largely simplified or even eliminated in practice, which increases the total radiated power and the efficiency of a wireless transmitter.

The matched radiation patterns are used in this paper just as a means to demonstrate the capabilities of the DFA and facilitate its future adoption. However, there is no fundamental limitation that restricts our DFA only to the antenna pattern similar to SFA. In fact, our proposed DFAs or in general MFAs offers large design/operation flexibilities and can achieve more versatile patterns than static SFAs.

2.3.3 *Modulation Measurement Results*

High data rates are crucial for 5G wireless communications and modulation test performance is the direct proof for how much and how fast information can be conveyed through the communication link. Therefore, wireless modulation test with broadside radiation is performed on both 38.5 and 73.5 GHz designs to demonstrate high-speed modulations in dynamic operations. Both 16QAM and 64QAM are used in the modulation tests. Conventional SFAs are also measured for performance comparison purpose. Loop-back test using two identical horn antennas is first conducted for measurement setup characterization and link calibration.

2.3.3.1 38.5-GHz Modulation Test

The setup for the 38.5-GHz modulation test is shown in Figure 2-26. The input baseband data are generated by an AWG and up-converted to 38.5 GHz by a mixer and an

image rejection filter. The LO of the mixer is provided by the signal generator. The up-converted signal is amplified through an RF amplifier and then sent to the antenna under test for transmitting. The transmitting signal is received by the horn antenna at far field, down-converted to 3 GHz, amplified by an IF amplifier and analyzed by an oscilloscope. The two signal generators are synchronized together through 10-MHz reference.

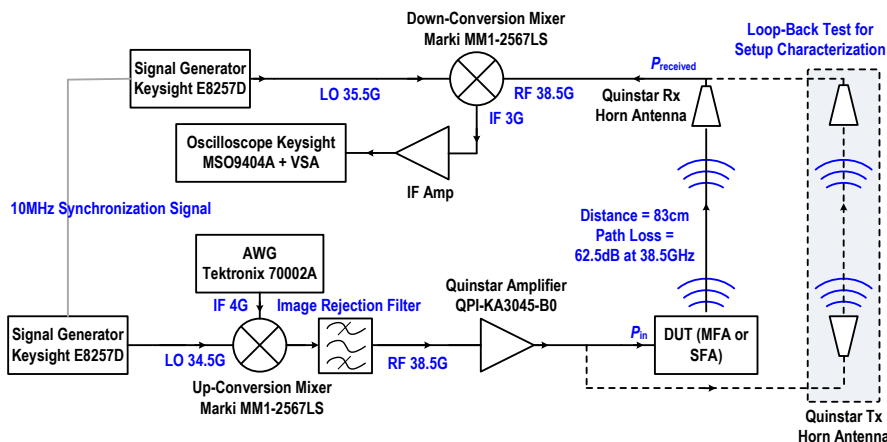


Figure 2-26 38.5-GHz modulation test setup.

Figure 2-27 summarizes the 0.5GSym/s 16QAM and 64QAM modulation results at 38.5 GHz, including error vector magnitude (EVM), constellation and adjacent channel leakage ratio (ACLR). For the 16QAM, the proposed dual-feed square loop antenna achieves an EVM of 3.4% with an ACLR of -33.3 dBc. Similar EVM and ACLR values are measured for the conventional SFA with 3.4% for EVM and -32.2 dBc for ACLR. For the 64QAM, 3.1% EVM and -32.6 -dBc ACLR are obtained by the DFA, with 2.9% EVM and -32.8 -dBc ACLR by the SFA. Close modulation performance is achieved by the proposed DFA, compared with the conventional SFA, proving that the modulated information is well preserved in the dual-feed configuration.

To further demonstrate the advantage of large available bandwidth at mm-Wave 5G bands, 1GSym/s (6 Gb/s) 64QAM is also performed, with the modulation results shown in Figure 2-28. The DFA achieves almost the same modulation performance for 1GSym/s

64QAM signal, showing the potential of DFA to support complex and high-speed modulations at mm-Wave frequencies.

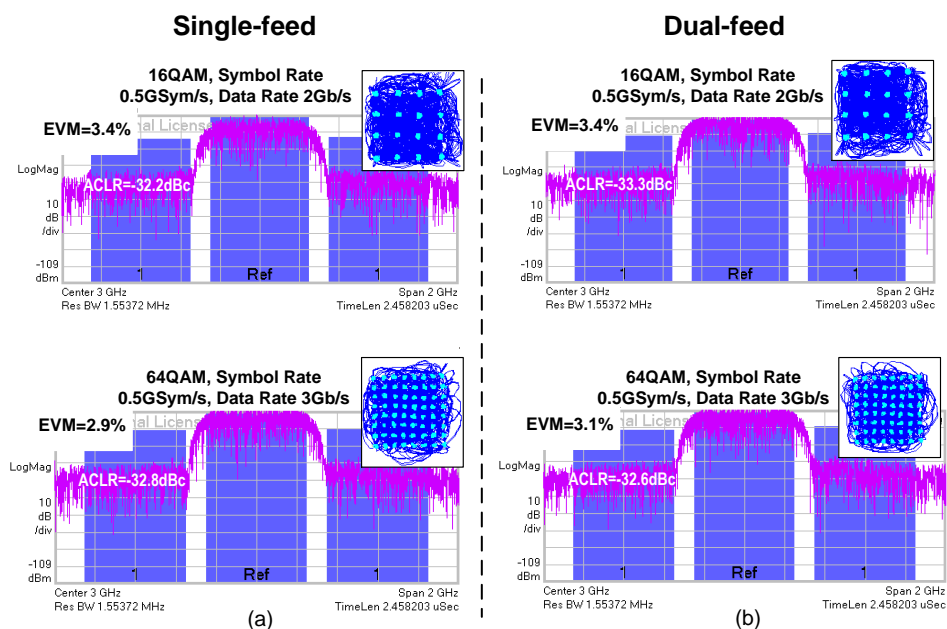


Figure 2-27 0.5GSym/s 16QAM and 64QAM modulation results at 38.5GHz of (a) SFA and (b) DFA.

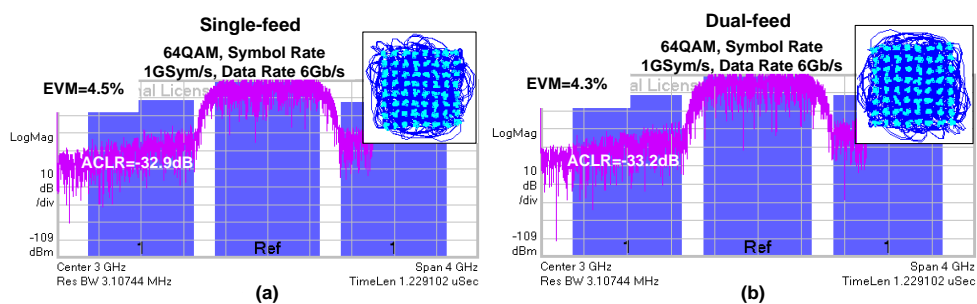


Figure 2-28 The 1GSym/s (6Gb/s) 64QAM result of the (a) conventional SFA and (b) proposed DFA at 38.5 GHz.

The measured EVMs of the DFA and SFA with complex modulations at different symbol rates are summarized in Figure 2-29. The EVM of the DFA closely tracks that of the SFA over different symbol rates for both 16QAM and 64QAM, which demonstrates the proposed DFA maintains the modulation capability of its conventional single-feed counterpart.

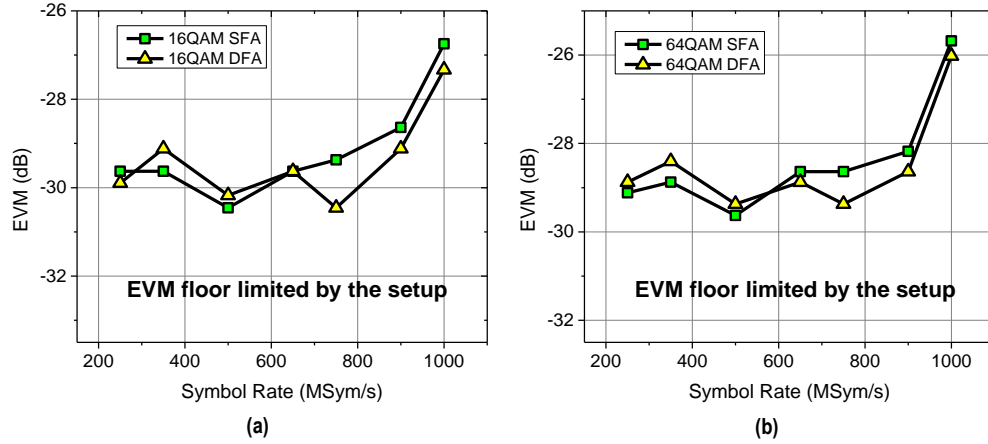


Figure 2-29 Measured EVM of the DFA and SFA versus symbol rate for (a) 16QAM and (b) 64QAM at 38.5 GHz.

2.3.3.2 73.5-GHz Modulation Test

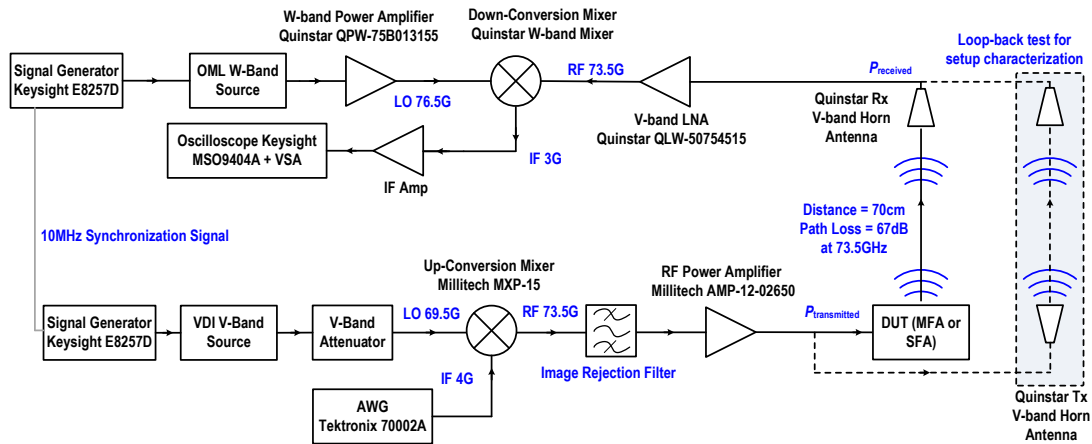


Figure 2-30 73.5-GHz modulation test setup.

The modulation test setup for the 73.5 GHz is shown in Figure 2-30. The LO signal of the up-conversion mixer is provided by a V-band source module. The input baseband data are generated by an AWG, up-converted to 73.5 GHz, amplified through an RF amplifier and then sent for transmitting. The received signal first goes through the V-band LNA to improve the noise figure of the demodulated path and increase the receiver dynamic range. The OML W-band source together with the W-band PA is implemented to provide enough LO power to drive the down-conversion mixer. The received RF signal is

down-converted to 3 GHz, amplified by the IF amplifier and eventually demodulated by the oscilloscope.

Figure 2-31 summarizes the 0.5GSym/s 16QAM and 64QAM modulation results at 73.5 GHz. For the 16QAM, the proposed dual-feed square loop antenna achieves an EVM of 4.9% with an ACLR of -33.1 dBc. Similar EVM and ACLR values are also measured for the conventional SFA with 4.6% for EVM and -32.4 dBc for ACLR. For the 64QAM, 4.1% EVM and -32.6 dBc ACLR are obtained by the DFA, with 4.1% EVM and -32 -dBc ACLR by the SFA.

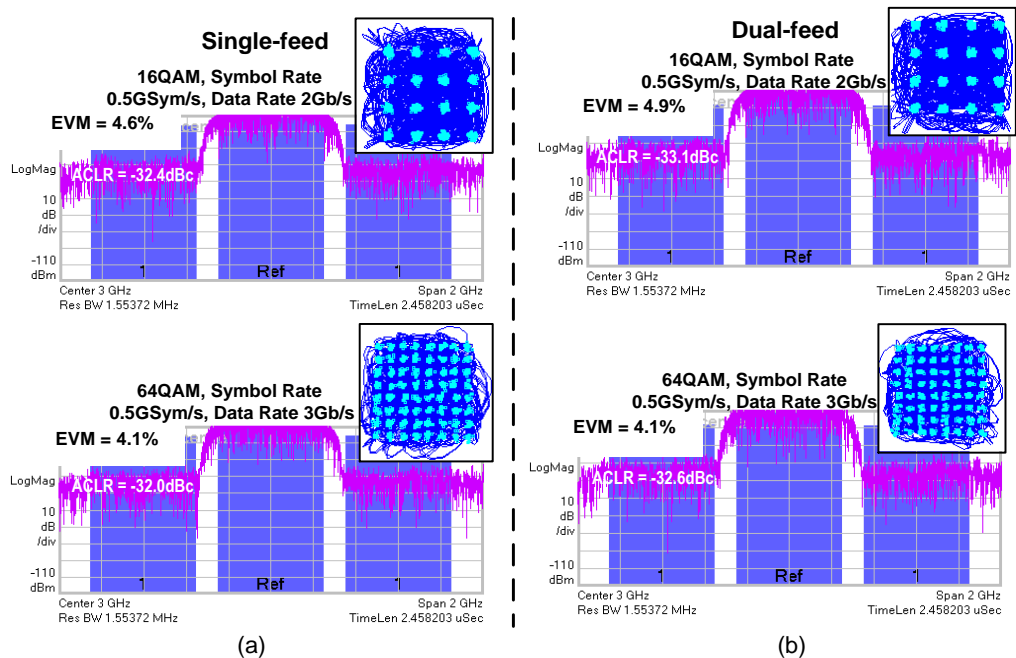


Figure 2-31 0.5GSym/s 16QAM and 64QAM modulation results at 73.5 GHz of (a) SFA and (b) DFA.

The modulation results of 1GSym/s (6 Gb/s) 64QAM at 73.5 GHz is shown in Figure 2-32. The DFA achieves almost the same modulation performance for 1GSym/s 64QAM signal at 73.5 GHz as well. Note that the modulation test results are currently limited by the setup.

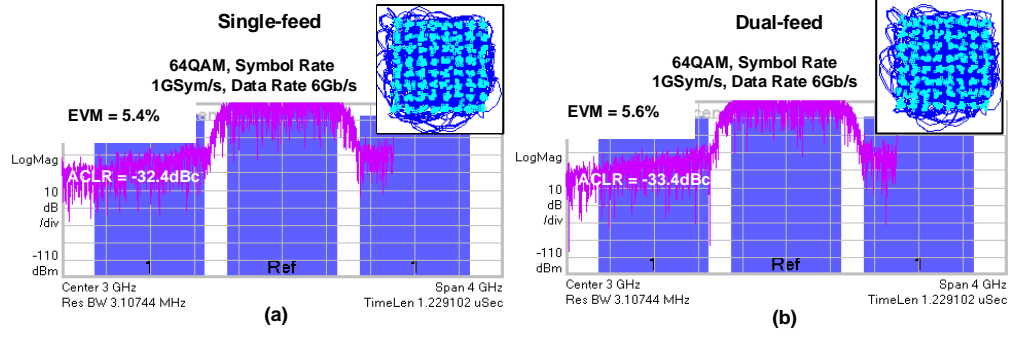


Figure 2-32 1GSym/s (6Gb/s) 64QAM result of the (a) conventional SFA and (b) proposed DFA at 73.5 GHz.

The measured EVM at 73.5 GHz with complex modulations at different symbol rates is shown in Figure 2-33. For both 16QAM and 64QAM, the EVM of the proposed DFA matches closely with that of the conventional SFA, showing the capability of the proposed DFA to support high data-rate communications at mm-Wave frequencies.

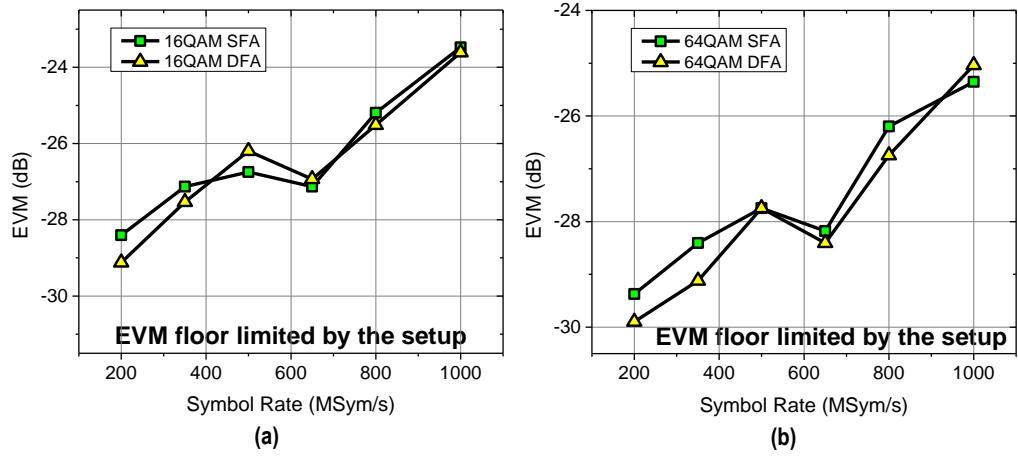


Figure 2-33 Measured EVM of the DFA and SFA versus symbol rate for (a) 16QAM and (b) 64QAM at 73.5 GHz.

The testing results in Figure 2-28 and Figure 2-32 show a higher data rate but a slightly degraded EVM. Since the conventional SFA and proposed DFA exhibit similar measured EVM values, this shows that the EVM degradation at a higher data rate is mostly due to measurement setup limitation.

The above modulation tests demonstrate the antenna performance when implemented in a transmitter. It not only achieves efficient on-antenna power combining, alleviating the difficulty of high-power generation at mm-Wave, but also provides sufficient bandwidth to meet the high data throughput requirement for 5G communications, offering significant improvements in channel capacity and boosting user data rates to accommodate rapidly increasing traffic demands of the future.

2.3.4 Conclusion

This section proposes an mm-Wave dual-feed square loop antenna that synthesizes identical antenna characteristics as the conventional SFA. The proposed antenna is able to achieve direct on-antenna power combining, without extra lossy power combining network between the transmitter and antenna. Such approach significantly improves the total radiated power and thus enhances the power efficiency of a wireless transmitter, which makes it not only suitable for high-power applications but also beneficial for portable devices to extend the battery life. Compared with antenna-array-based spatial power combining, it only requires a single-antenna footprint, being a more cost-effective solution. More importantly, antenna array suffers from narrowed beamwidth, but the proposed antenna maintains the single-element antenna beamwidth; therefore, it poses less challenge on the Tx/Rx alignment, ideal for dynamic and mobile applications. Inherent antenna impedance down-scaling is also realized in the presented antenna design. It greatly eases the design of the PA, especially helpful for high-power applications. The dual-feed square loop antenna is designed and characterized at two potential 5G bands, centered at 38.5 and 73.5 GHz. Conventional single-feed square loop antennas are also implemented as reference designs. Closely matched antenna characteristics are achieved in measurement between the proposed DFAs and conventional SFAs. The dual-feed square loop antenna has measured broadside gain of 2.9 and 3 dBi, fractional bandwidth of 13% and 14%, at 38.5 and 73.5 GHz, respectively. High-speed modulation test is also performed using the

proposed antennas. A 4.3% EVM with a -33.2 dBc ACLR for 6-Gb/s (1GSym/s) 64QAM is achieved at 38.5 GHz, and a 5.6% EVM with a -33.4 dBc ACLR for 6 Gb/s (1GSym/s) 64QAM is measured at 73.5 GHz, which demonstrates the viability of the proposed antenna to support high-speed and complex modulation schemes required by 5G communications.

CHAPTER 3. A MM-WAVE FLIP-CHIP PACKAGED CHIREIX TRANSMITTER WITH ON-ANTENNA OUTPHASING ACTIVE LOAD MODULATION

3.1 Introduction

The exponential growth in data rates for modern wireless communication demands greater bandwidth for the upcoming 5G wireless systems. Millimeter-wave (mm-Wave) offers broader available spectrums and proportionate increase of channel capacity. Therefore, it is leveraged in 5G systems to address the increasing demands for fast data speed and low network latency. It also enables large-scale beamforming to compensate the high path loss at mm-Wave. Viable mm-Wave transmitter (TX) frontend solutions should handle multi-Gb/s spectrum-efficient modulated signals, such as high-order quadrature amplitude modulations (QAMs). Their corresponding large peak-to-average power ratios (PAPRs) place a demanding requirement on both peak and power back-off (PBO) efficiency to guarantee a high average efficiency in modulation. Moreover, high system power efficiency is of paramount importance to reduce cooling needs in massive multiple-input-multiple-output (MIMO) and large-scale phased-array systems, which will significantly reduce maintenance cost and ease system deployment.

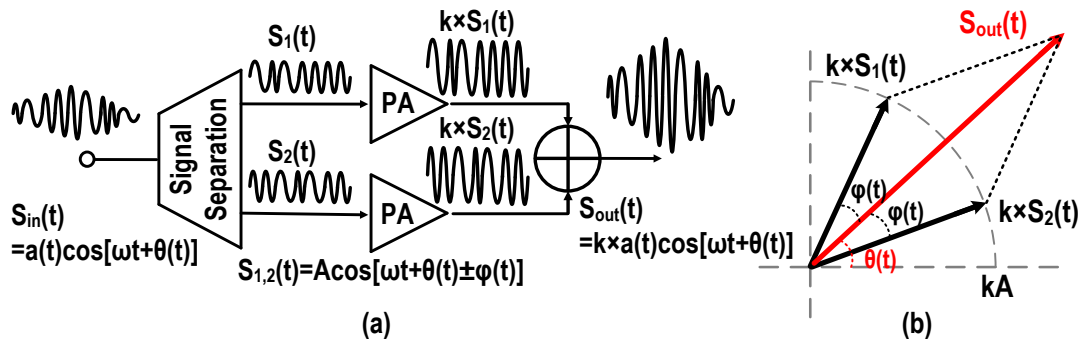


Figure 3-1 (a) Outphasing architecture, and (b) its vector representation.

Mm-Wave Doherty TX/PA is a widely used technique to enhance PA PBO efficiency [22]-[26]. However, many existing Doherty TX/PA designs exhibit either compromised peak efficiency [22] or limited efficiency improvement at PBO [24], largely due to the lossy mm-Wave Doherty power combiners and imperfect Doherty operations. Outphasing is an alternative and popular solution to achieve large PBO efficiency enhancement while maintaining a high peak efficiency. A typical outphasing architecture is composed of two PAs that operate with saturated envelope but dynamically varying phase difference, to synthesize the desired envelope varying complex modulation signals (Figure 3-1). Due to the saturated PA operations, outphasing TXs maximize the output power (P_{out}) range towards the saturated output power (P_{sat}) and thus maximize the TX efficiency [27]-[36]. Moreover, rapid advance in baseband processors using deeply scaled CMOS reduces digital computation power for outphasing signal generations. In large-scale array systems, one modulator can also be shared among multiple TX/PA units to further reduce the computation power. As a result, outphasing is an attractive and potential candidate for 5G TX/PA architectures to achieve large-scale, energy-efficient, and agile beamforming.

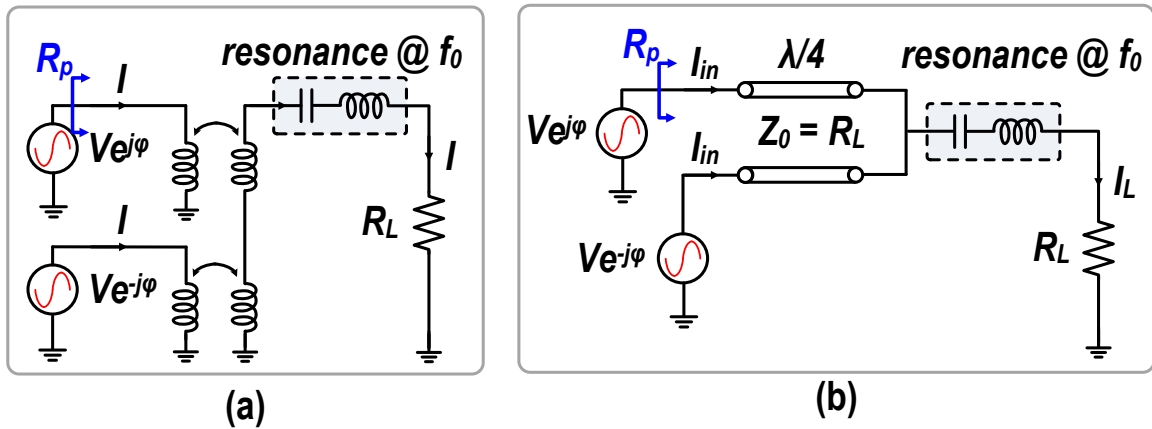


Figure 3-2 Non-isolating outphasing combiner using (a) transformers and (b) $\lambda/4$ transmission lines.

However, a major remaining challenge is the lack of non-isolating outphasing power combiners at mm-Wave that have low loss and support desired active load modulation behavior, making high performance mm-Wave outphasing TX/PA still a challenging task [31], [36]. In essence, non-isolating outphasing combiners are series power combining networks. Two general outphasing combiner schematics are shown in Figure 3-2. The series power combining nature of outphasing performs voltage summation at the output, which are typically implemented as transformers or $\lambda/4$ transmission line-based combiners (Figure 3-2). Transformers at mm-Wave introduce significant leakage inductance and parasitic capacitance, making their behaviors as well as impedance balancing far from ideal series power combiners. Additionally, limited quality factor makes the transformer-based outphasing combiner quite lossy at mm-Wave (e.g., 1.2dB in [31]). As a result, the desired outphasing active load modulation is largely compromised, which leads to marginal efficiency improvement at PBO. On the other hand, $\lambda/4$ transmission line-based series power combiners occupy a significant chip footprint at low/medium mm-Wave (28GHz), which is not practical for an on-chip implementation. Therefore, a new type of high-efficiency series power combiner that support desired active load modulation is in great need to realize high performance mm-Wave outphasing TX/PA.

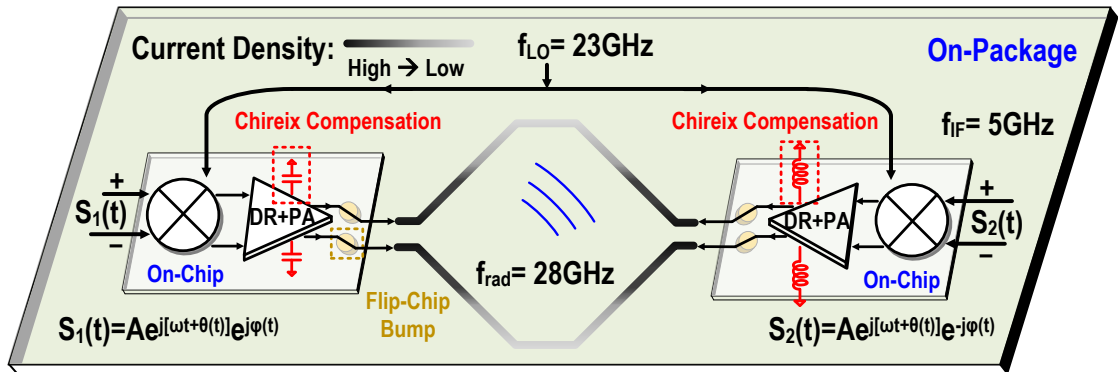


Figure 3-3 Top-level schematic of the Chireix transmitter.

To address this difficulty, a 28-GHz packaged Chireix TX solution is proposed with direct on-antenna outphasing load modulation [37]. The Chireix TX contains two 28-GHz phase-shifted sub-TXs simultaneously driving a dual-feed loop antenna (DLA) on package (Figure 3-3), which achieves high-efficiency on-antenna outphasing load modulation. This chapter will show that a DLA naturally serves as a non-isolating outphasing power combiner, demonstrating superior active load modulation and low loss over conventional on-chip outphasing passive networks. Moreover, DLA offers built-in antenna impedance down-scaling at each feed due to its series power combining nature and greatly simplifies the matching interface between antenna and PAs [2], [3], [5]. To further improve the TX efficiency and its dynamic range, Chireix compensation and a hybrid outphasing operation are also incorporated into this design [38], [39], whose details will be presented in this paper.

3.2 Design Details of the 28-GHz Chireix Transmitter

The proposed two-way Chireix TX contains two 28-GHz phase-shifted sub-TXs driving one DLA on package. Each Chireix sub-TX circuit consists of an up-conversion double balanced mixer and a two-stage PA (Figure 3-3). The two sub-TX chips are integrated with the DLA by flip-chip packaging for minimized interconnection parasitic. With antenna serving as both a radiator and a power combiner, direct on-antenna power combining, and unique antenna-level active load modulation are realized. The corresponding design methodology and detailed circuit implementation are presented in this section.

3.2.1 Ideal Non-Isolating Power Combiners

Non-isolating power combiners introduce interactions between the two outphasing paths to achieve active load modulations for efficiency enhancement at PBO, which cannot

be realized by isolating power combiner. As two popular examples, the transformer-based and $\lambda/4$ line-based non-isolating combiners are shown in Figure 3-2. In Figure 3-2 (a), when driven by two outphased voltage sources ($Ve^{j\varphi}$ and $Ve^{-j\varphi}$), the output currents of the power devices at f_0 can be obtained as

$$I = \frac{Ve^{j\varphi} + Ve^{-j\varphi}}{R_L} = \frac{2V\cos(\varphi)}{R_L}. \quad (3-1)$$

The output power (P_L) and parallel load resistance (R_p) for each PA branch are derived as

$$P_L = \frac{1}{2}I^2R_L = \frac{2V^2\cos^2(\varphi)}{R_L}, \text{ and} \quad (3-2)$$

$$R_p = \frac{1}{\text{Re}(\frac{I}{Ve^{\pm j\varphi}})} = \frac{R_L}{2\cos^2(\varphi)}. \quad (3-3)$$

Thus, load resistance R_p increases at PBO when φ increases from 0° to 90° , which describes the desired outphasing active load modulation and thus ensures PBO efficiency enhancement.

The same conclusion can be drawn using the $\lambda/4$ combiner network in Figure 3-2(b). The $\lambda/4$ T-lines convert the input voltage $Ve^{\pm j\varphi}$ into current $-jVe^{\pm j\varphi}/Z_0$. The currents from the two branches are then summed at the load. Alternatively, one can recognize that the two $\lambda/4$ T-lines and a shunt branch is equivalently a series power combiner. The resulting load current through R_L is

$$I_L = -\frac{jVe^{j\varphi} + jVe^{-j\varphi}}{Z_0} = -j\frac{2V\cos(\varphi)}{R_L}. \quad (3-4)$$

Therefore, the load voltage is expressed as

$$V_L = -j2V\cos(\varphi). \quad (3-5)$$

The currents injected into the combiner network can be determined as

$$I_{in} = j \frac{V_L}{Z_0} = \frac{2V\cos(\varphi)}{R_L} \quad (3-6)$$

which follows the same relationship in (3-1). As a result, the active load modulations described in (3-2) and (3-3) are realized in this case as well.

3.2.2 On-Antenna Outphasing Active Load Modulation

Despite the desired operation of idealistic non-isolating outphasing power combiners (Figure 3-2), the absence of a low-loss effective mm-Wave non-isolating power combiner in practice largely impedes the implementation of outphasing architectures. To address this challenge, a DLA is exploited as an outphasing power combining network. When driven by two outphasing signals, common- and differential-mode analyses can be applied to study the proposed network (Figure 3-4).

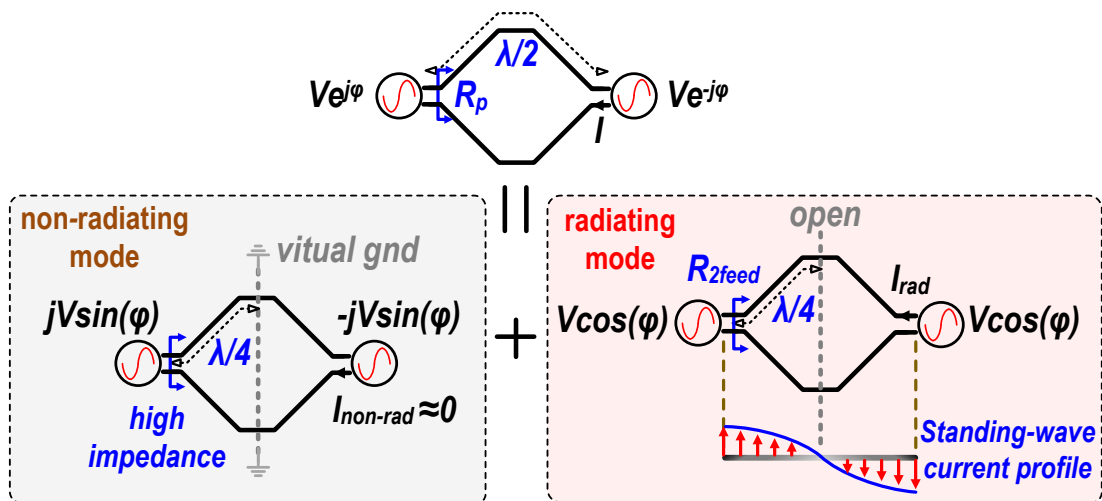


Figure 3-4 Proposed on-antenna outphasing power combiner.

The differential-mode components ($\pm jV\sin\varphi$) of the input signals ($Ve^{\pm j\varphi}$) result in the non-radiating mode of the antenna. A virtual ground is formed in the middle of the DLA due to the differential excitations. The $\lambda/4$ arms of the antenna then transform the virtual ground to the high impedance ($3.4 \text{ k}\Omega$ in simulation) at the antenna feeds. As a result, negligible RF current flows into the network in this undesired non-radiating/differential mode.

On the other hand, the common-mode signals ($V\cos\varphi$) of the outphasing sources excite the desired radiating mode of the antenna, and lead to low input impedance R_{2feed} . The total RF current on the antenna is thus only determined by the desired radiating common mode, and is described as

$$I = I_{rad} + I_{non-rad} \approx I_{rad} = \frac{V\cos(\varphi)}{R_{2feed}}. \quad (3-7)$$

In addition, DLA offers built-in antenna impedance downscaling at each feed due to its series power combining nature ($R_{2feed} = R_{rad}/2$) [5]. Hence (3-7) can be further expressed as

$$I = \frac{2V\cos(\varphi)}{R_{rad}}, \quad (3-8)$$

where R_{rad} is the radiation impedance of an identical loop antenna but with a standard single feed. As a result, the P_L and R_P in the proposed DLA can be obtained as

$$P_L = 2 \times \frac{1}{2} I^2 R_{2feed} = \frac{2V^2 \cos^2(\varphi)}{R_{rad}}, \text{ and} \quad (3-9)$$

$$R_p = \frac{1}{\text{Re}(\frac{I}{V_{e^{\pm j\varphi}}})} = \frac{R_{rad}}{2\cos^2(\varphi)}. \quad (3-10)$$

Comparing (3-9) and (3-10) with (3-2) and (3-3), the DLA achieves the same load modulation behavior as an ideal non-isolating outphasing power combiner, with the load R_L in the ideal conventional combiner replaced by the radiation impedance R_{rad} in the proposed DLA power combining structure.

This theoretical derivation is further verified by 3-D EM simulation results in Figure 3-5 Comparison of active load modulation between EM-simulated on-antenna outphasing network and ideal power combiner.. The active load modulation achieved using the proposed DLA as the combiner (R_{P_EMsim}) matches well with that realized by the ideal power combining network (R_{P_ideal}). The small discrepancy between R_{P_ideal} and R_{P_EMsim} is due to the finite differential-mode driving impedance of the DLA. Thus, the normalized power delivered to the antenna (P_{L_EMsim}) closely follows the theoretical $\cos^2\varphi$ relationship as indicated in (3-2) and (3-9), shown in Figure 3-5.

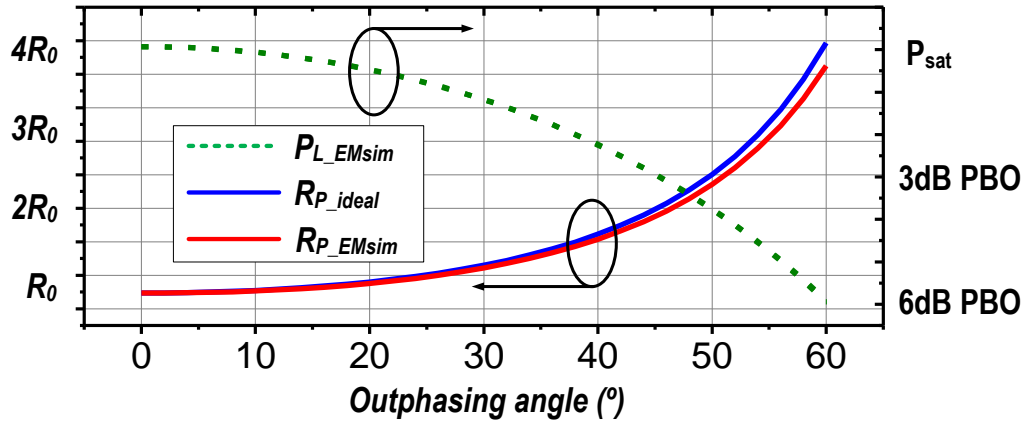


Figure 3-5 Comparison of active load modulation between EM-simulated on-antenna outphasing network and ideal power combiner.

The antenna EM structure, simulated antenna pattern, driving impedance at each feed (Z_{in}), and bandwidth are shown in Figure 3-6. The DLA is designed on a 20-mil-thick RO4350 substrate with dimensions of 3.5 mm by 2.5 mm [Figure 3-6(a)]. Including the flip-chip transition, the on-package DLA is designed to radiate at the target 28 GHz, and offer radiation impedance as the PA optimum load impedance R_{opt} , which directly simplifies the PA output matching.

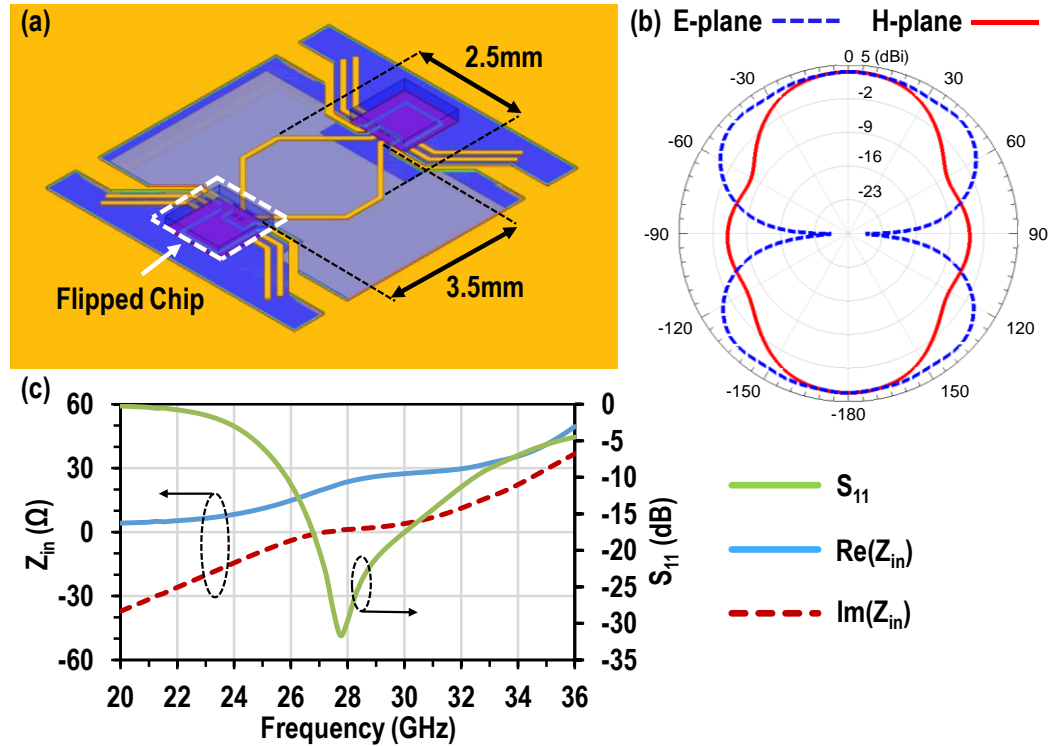


Figure 3-6 (a) Dual-feed antenna EM model. (b) Antenna radiation pattern at $\varphi = 0^\circ$. (c) Antenna input impedance and impedance bandwidth.

The impact of packaging variations on the antenna impedance is also simulated and plotted in Figure 3-7(a). The nominal dimension of a flip-chip bump is 50 μm in both diameter and height. The desired common-mode impedance remains relatively constant, considering 50- μm variation in the bump diameter (50–100 μm) and height (30–80 μm).

The antenna radiation/passive efficiency is 95% at 28 GHz, with a boresight antenna gain of 3.1 dBi [Figure 3-6(b)]. The gain value is later used to calibrate the PA output power. The EM simulated antenna common-mode single-ended impedance is $23\ \Omega$ at 28 GHz [Figure 3-7(a)], while the differential-mode impedance is $3.4\ \text{k}\Omega$ [Figure 3-7(b)], verifying that the differential mode is the non-radiation mode.

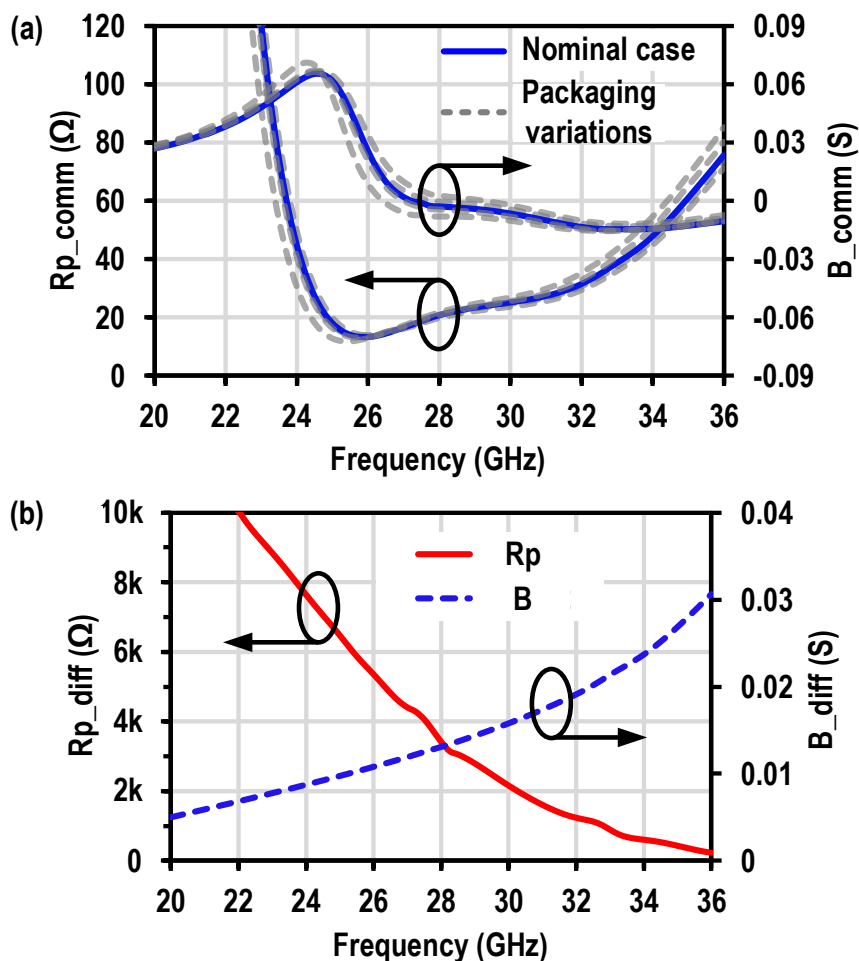


Figure 3-7 (a) Desired common-mode antenna impedance under packaging variations. (b) Differential-mode antenna impedance.

3.2.3 Antenna Response to Outphasing

Since Sections 3.2.1 and 3.2.2 show that the on-antenna power combiner achieves identical outphasing active load modulation as an ideal non-isolating power combiner, the

antenna far-field behaviors under the outphasing driving conditions becomes the next question to answer. Because any change in the antenna characteristics (such as pattern and gain) induced by the outphasing operation will corrupt the demodulated signals at the far-field receiver (RX) end.

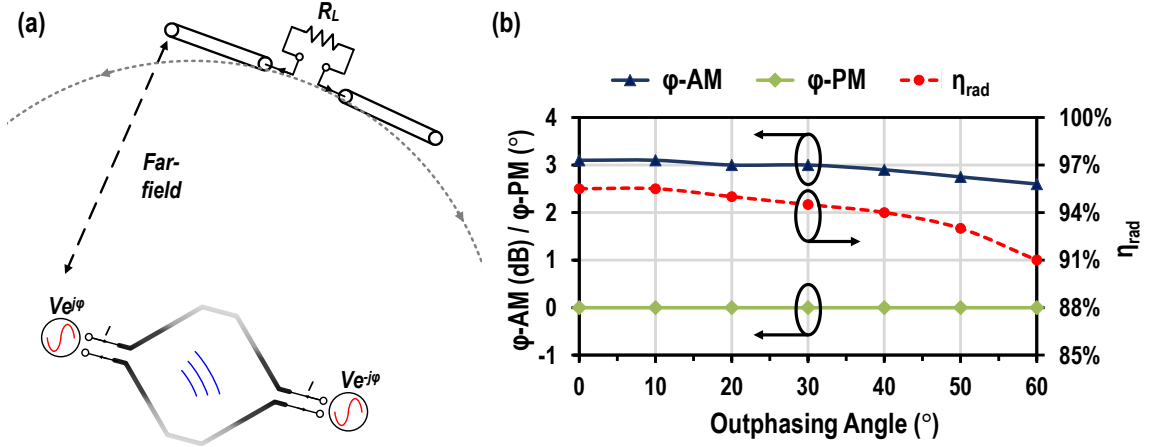


Figure 3-8 (a) Far-field nonlinearity characterization setup of the on-antenna combiner. (b) Simulated amplitude and phase response to outphasing operation.

Unlike conventional TXs whose output power is combined and delivered to a fixed load, the multi-feed antenna processes the distributed transmitted power from its feeds and finally radiates it out. Since the on-antenna processing is not performed independently at each antenna feed, circuit performance parameters (P_{out} , AM-AM, AM-PM, etc.) should be examined at the target RX antenna load in the far-field, so that the complete on-antenna operations and channel non-idealities are captured. Since the input AM is decoded as the offset angle φ in outphasing, a simulation test setup [Figure 3-8(a)] is built to quantify the φ -AM and φ -PM linearities of the outphasing TX chain. A dipole antenna is implemented as the target far-field RX, with the DLA driven by the outphasing signals as the TX.

Ideally, the antenna pattern and gain should remain unaffected during the outphasing operation to maintain large-signal linearity at the far-field RX. The simulated φ -AM and φ -PM results are shown in Figure 3-8(b). To accurately quantify the

nonlinearities only caused by the proposed DLA, outphased voltage sources are used in this simulation to drive the DLA. Within 60° outphasing angle, the φ -AM variation is below 0.5 dB, with φ -PM remaining constant. The degraded φ -AM variation beyond 60° outphasing angle is mainly caused by the unwanted differential-mode radiation. The antenna radiation efficiency (η_{rad}) is also plotted in Figure 3-8(b), showing $>90\%$ η_{rad} during outphasing operation. It is worth noting that the large-signal linearity is preserved over the entire antenna field of view (FoV). Unlike the spatial IQ [40] and spatial outphasing technique [41], the proposed on-antenna outphasing maintains spatially independent signal integrity, which is further demonstrated in the measurement (Section 3.3.2).

In this design, we introduce a hybrid outphasing scheme (Section 3.2.6) to keep the outphasing angle below 60° and minimize φ -AM distortion induced by the antenna. Linear amplification is employed at deep PBO to improve the TX dynamic range and avoid the deep outphasing region ($60^\circ < \varphi < 90^\circ$), since perfect matching between the branches and thereby complete out-of-phase component cancelation is difficult to achieve in practice, which often constrains the dynamic range in conventional outphasing TXs.

3.2.4 TX Circuit Schematic

Each Chireix sub-TX circuit consists of an up-conversion double-balanced mixer and a two-stage PA. The antenna-based outphasing network combines the two paths and realizes active load modulation. The PA schematic is shown in Figure 3-9(a). Each PA path comprises a driver stage and a PA stage with capacitive neutralization to boost power gain and enhance device stability. High-Q differential inductors are added at the PA output to resonate out device capacitance and provide supply bias and Chireix compensation. The details of Chireix compensation is discussed in Section 3.2.5.

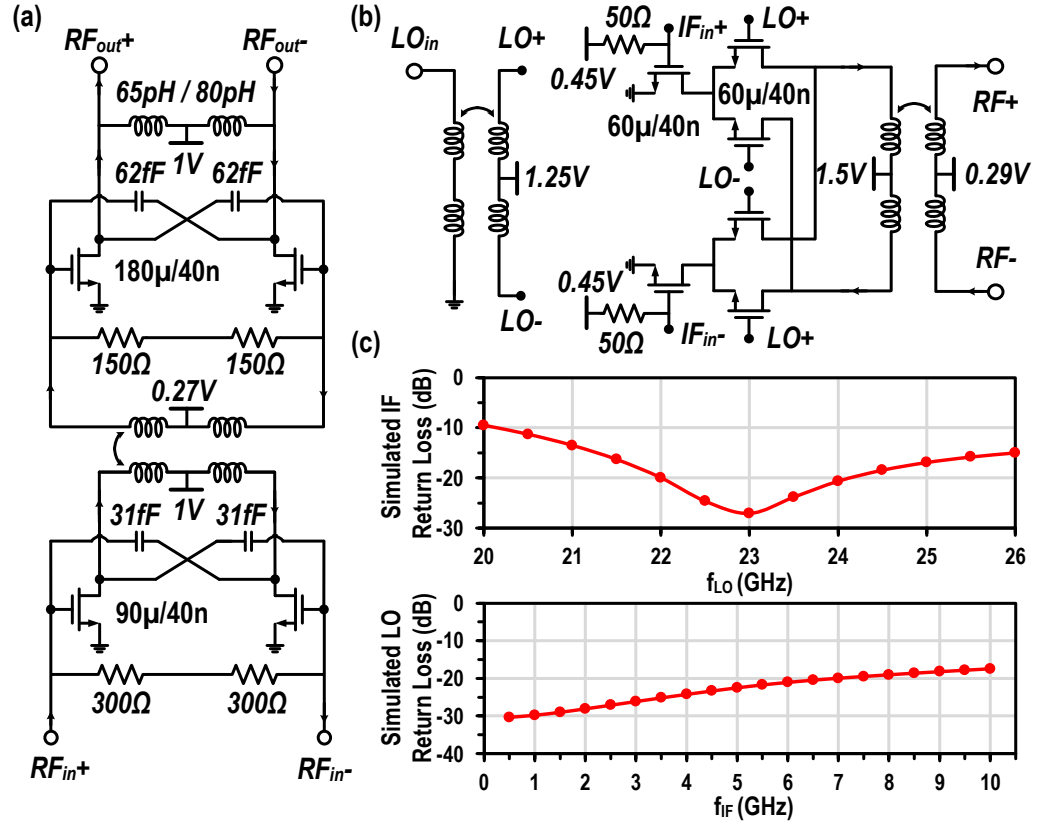


Figure 3-9 (a) Schematic of the two-stage TX PA. (b) Schematic of TX mixer. (c) Simulated mixer LO and IF return loss.

Double-balanced mixers up-converts the 5-GHz IF signals to the 28-GHz carrier. On-chip mixer implementation minimizes the phase/amplitude mismatch between the two outphasing paths. Figure 3-9(b) shows the mixer schematic with transformers as the inter-stage matching and LO balun. The simulated wideband matching is plotted in Figure 3-9(c). With 3-dBm LO driving strength, the mixer requires -7.5-dBm IF input power to fully saturate the PA.

Although typical outphasing PAs/TXs are analyzed assuming voltage sources driving (Figure 3-2), typical linear mm-Wave PAs exhibit appreciable output impedance at the operation frequency, leading to extra distortion and peak/PBO efficiency decrease in outphasing operations. An overdriven Class-B common-source (CS) PA is chosen as the

PA stage for its smaller output impedance and inherently higher device efficiency. Operating power gain (G_p) and large-signal output impedance (R_{out}) of a CS and cascode PA are compared in Figure 3-10(a). In both cases, the same device size is used, and the two PAs are loaded with their corresponding load-pull impedances.

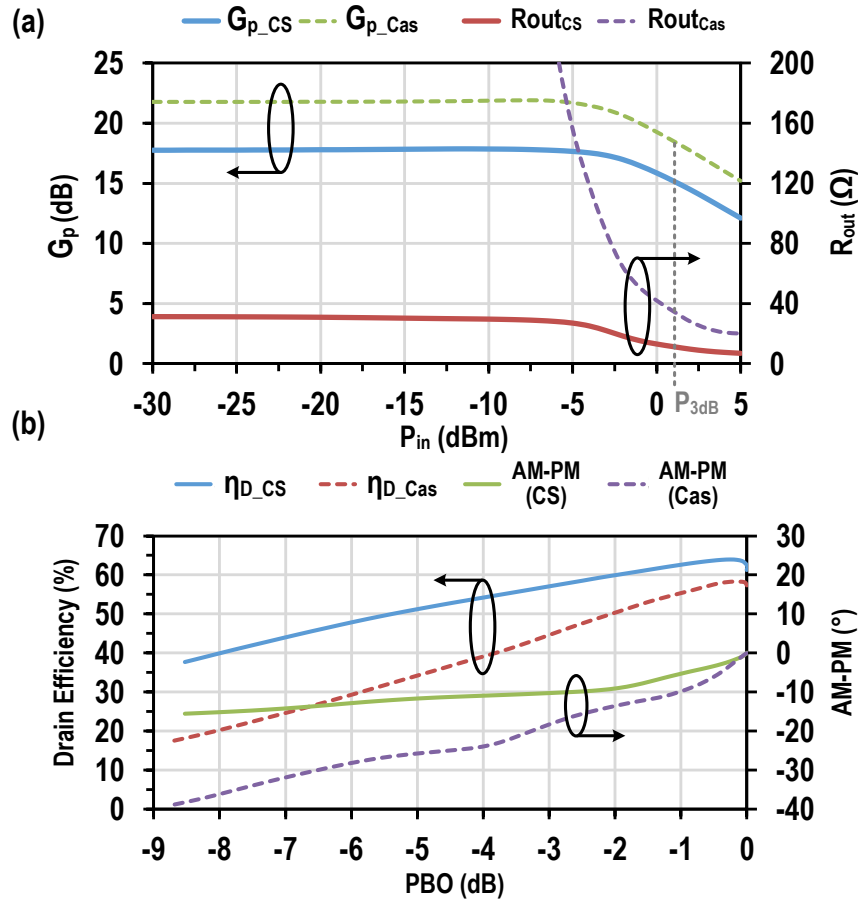


Figure 3-10 (a) G_p and R_{out} of CS and cascode PA versus input power. (b) Performance comparison between CS and cascode PA in outphasing operation.

At 3-dB compression point (where the device is largely saturated), the output impedance of the CS PA is 10 Ω that is much smaller than that of the cascode PA (39 Ω). Due to the low device output impedance of an overdriven CS PA, and its constant output voltage amplitude constrained by the transistor saturation, it is a good approximation of a voltage-source, desired for PBO efficiency enhancement in outphasing architecture. The

performance comparison between the CS and cascode PA in outphasing operations is summarized in Figure 3-10(b). The PAs are driven at the same constant input power level ($P_{in} = 2$ dBm) with increasing outphasing angle for PBO in the two cases. The implementation with the CS PA not only exhibits a higher peak efficiency but maintains a higher efficiency at PBO. Moreover, much less AM–PM distortion is observed with the CS PA, further demonstrating the advantage of using overdriven CS topology in outphasing. In this design, the PA is driven at the 3-dB compression point for maximum efficiency during the outphasing operation. The driver stage is biased in Class-AB and has half size of the PA stage to provide sufficient driving strength to saturate the PA.

3.2.5 Chireix Compensation

During the outphasing operation, not only the real load resistance R_p is being modulated, but also an associated reactive component is varying versus the outphasing angle [Figure 3-11(a)]. Revisiting the outphasing schematic in Figure 3-2, the reactive parts seen by each branch can be written as

$$Im(Y) = Im\left(\frac{I}{Ve^{\pm j\varphi}}\right) = \pm \frac{\sin 2\varphi}{R_L}, \quad (3-11)$$

$$L_p = -\frac{1}{\omega \times Im(Y)} = \frac{R_L}{\omega \times \sin 2\varphi}, \text{ for } Im(Y) < 0, \quad (3-12)$$

$$C_p = \frac{Im(Y)}{\omega} = \frac{\sin 2\varphi}{\omega \times R_L}, \quad \text{for } Im(Y) > 0, \quad (3-13)$$

Therefore, one outphasing path sees an inductive load, while the other observes a capacitive load. It should be noted that the use of saturated linear PAs (such as Class-B) cannot cope with such power-dependent reactive load impedances, leading to substantial PBO efficiency degradation. Thus, Chireix compensations are needed to cancel out the reactive

loads at a predefined outphasing angle for better efficiency enhancement at PBO [27]–[29]. Theoretical PA efficiency (η) with a Chireix power combiner is derived as [28], [30], [34]

$$\eta = \frac{2\cos^2\varphi}{\sqrt{(2\cos^2\varphi)^2 + (\sin 2\varphi - \sin 2\varphi_c)^2}} \quad (3-14)$$

where φ_c is the predefined compensation angle. By substituting (3-2) into (3-14), the relationship between η and P_L is obtained and plotted in Figure 3-11(b). Without any compensation, the PA efficiency rolls off rapidly during the PBO. By choosing different compensation angles (φ_c), the efficiency can be optimized at the corresponding PBO level.

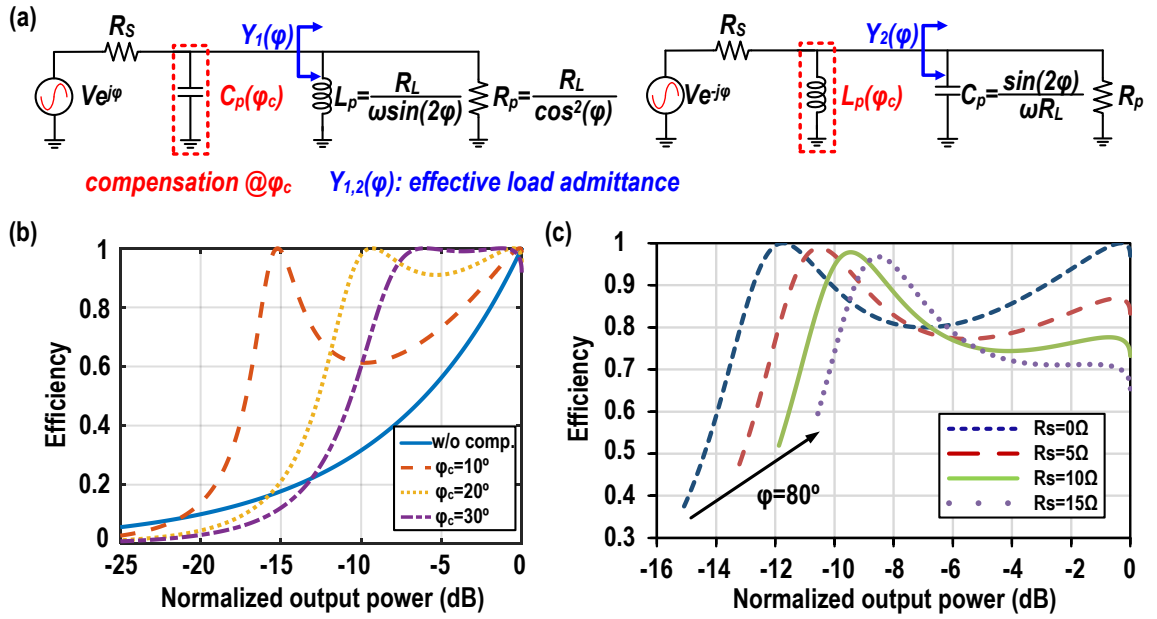


Figure 3-11 (a) Equivalent circuit for the two outphasing paths. (b) Chireix combiner efficiency at power back-off with zero source resistance (R_s). (c) Chireix combiner efficiency at power back-off with different R_s values.

The above analysis assumes ideal voltage sources with zero source resistance (R_s). For a practical design, the effect of R_s should be evaluated. Figure 3-11(c) shows the influence of R_s on the efficiency for the same Chireix compensation angle ($\varphi_c = 15^\circ$) with lossless passives. All the four curves are plotted up to the PBO level with a maximum

outphasing angle of $\varphi = 80^\circ$. Shown in Figure 3-11 (c), larger R_S value directly degrades the peak efficiency. Moreover, the second efficiency peak moves to a smaller PBO level with a larger R_S . In addition, the dynamic range is also reduced by a larger R_S for the same maximum outphasing angle. These observations further explain why a lower PA output impedance is preferred in an outphasing architecture, justifying the use of overdriven Class-B CS PAs. In this design, a 15° compensation angle is chosen to optimize the TX average efficiency when transmitting 64-QAM signals.

It is worth noting that the ideal symmetry of outphasing architecture no longer holds by adding the reactive Chireix compensation [29], [42]. This is due to the non-zero R_S of the voltage sources. In this case, the peak output power (0-dB PBO) is achieved at a shifted outphasing angle φ_0 , rather than at $\varphi = 0^\circ$. The output power is now given by a modified relationship as

$$P_L = \frac{2V^2}{R_L} \times \frac{1 + 2(R_S B_C)^2}{\left(1 + \frac{2R_S}{R_L} + R_S^2 B_C^2\right)^2} \cos^2(\varphi - \varphi_0) \quad (3-15)$$

where $\varphi_0 = \tan^{-1}(B_C R_S)$ and $B_C = \sin 2\varphi_C / R_L$. Compared with (3-2) for an ideal outphasing case, the relationship shown in (3-15) implies that constant phase shift and magnitude scaling should be considered for outphasing signal generation.

3.2.6 Hybrid Outphasing Operation

As presented in Section 3.2.3, the outphasing angle is kept within 60° (corresponding to 6-dB PBO) for better linearity and dynamic range. Within this 6-dB PBO, the TX input power is reduced gradually. First, due to the increasing load at the increasing outphasing angle, less input power is actually required to drive the device into saturation [38], [43], [44]. Moreover, this gradually decreasing input power reduces the PA

gain compression and improves the PA power-added efficiency (PAE). Beyond 6-dB PBO, the TX is operating in its linear operation mode where only input amplitude is being decreased with the outphasing angle fixed at 60° . The complete hybrid outphasing operation is illustrated in Figure 3-12. Similar principles but with mixed-mode operations have also been applied in [38] and [39] for GHz implementations.

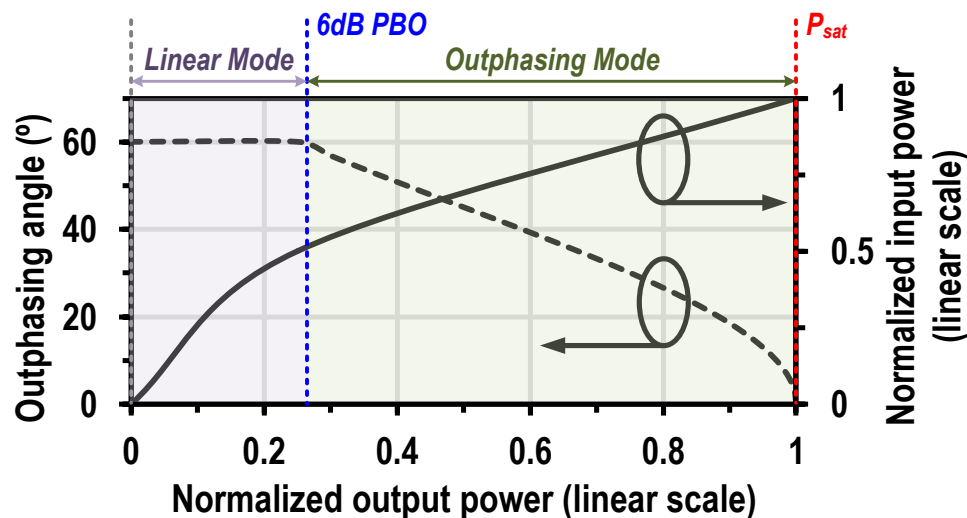


Figure 3-12 Hybrid outphasing operation principle.

3.3 Measurement Results

The 28-GHz Chireix TX IC chips are fabricated in GlobalFoundries 45-nm CMOS SOI process. Two sub-TX chips are flip-chip packaged with the on-package antenna. A separate PA test structure (TS) is also implemented in the same process for accurate power characterization. Figure 3-13 shows the photograph of the fully packaged TX module, the X-ray image of the flip-chip transitions, and micrographs of the TX chip and PA TS.

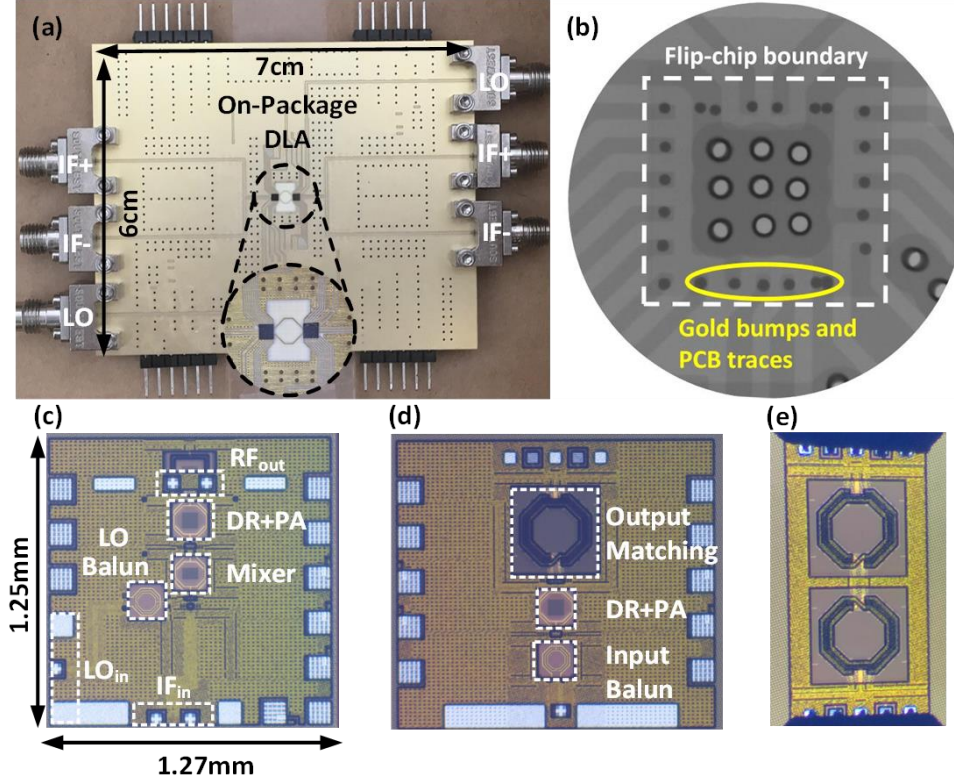


Figure 3-13 (a) Fully packaged Chireix TX module. (b) X-ray image for verification of flip-chip transition alignment. (c) Sub-TX die photograph. (d) PA standalone TS. (e) Back-to-back TS of OMN of PA TS.

3.3.1 Continuous-Wave Measurement

Figure 3-14(a) depicts the CW measurement setup. Two channels from the arbitrary waveform generator (AWG) are used to generate the desired outphasing signals at IF (5 GHz), with a signal generator providing the LO (23 GHz) input for the two chips. A horn antenna is placed at the far-field (83 cm) to receive the radiated CW signal, and a power sensor measuring the received power (P_r). The Equivalent Isotropically Radiated Power (EIRP) of the TX can then be calculated by de-embedding the PL and RX antenna gain (G_{horn}), as

$$EIRP = P_r - G_{horn} + PL. \quad (3-16)$$

The output power (P_{out}) of the Chireix TX is defined as the total power delivered to the antenna. Two approaches are employed to achieve accurate Chireix TX P_{out} measurement.

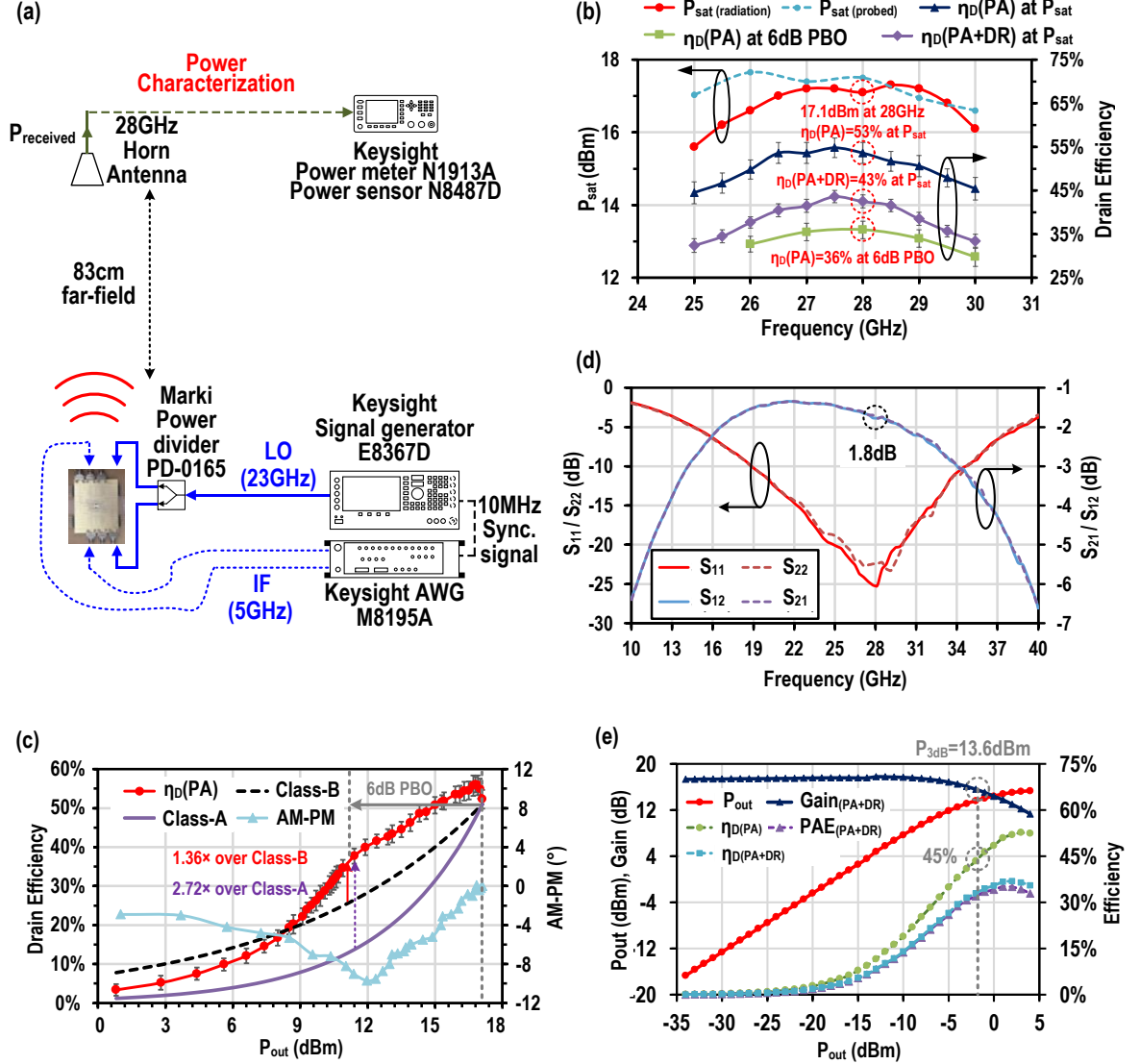


Figure 3-14 (a) CW measurement setup. (b) Chireix TX performance over frequencies. (c) PA large signal behaviors at 28 GHz. (d) S-parameters of the back-to-back PA TS OMN. (e) PA TS large signal performance at 28 GHz.

It can be attained by subtracting the TX outphasing antenna gain (G_{ant}) from the EIRP, as

$$P_{out} = EIRP - G_{ant}. \quad (3-17)$$

The P_{out} based on the measured EIRP and EM simulated Gant is plotted in Figure 3-14(b), yielding a 17.1-dBm P_{sat} at 28 GHz with 53% PA-stage drain efficiency (DE) (η_D). Including the driver power consumption, the total PA $\eta_D(\text{PA}+\text{DR})$ is 43% (\approx PAE, considering >15-dB two-stage PA power gain). The P_{sat} 1-dB bandwidth covers from 25.5 to 30 GHz, while maintaining at least 45% $\eta_D(\text{PA})$ and 34% $\eta_D(\text{PA}+\text{DR})$. The PA large-signal behaviors at 28 GHz are summarized in Figure 3-14(c). Four independent measurements on two different TX modules have been performed. Based on these measurements, the standard deviation on the measured PA DE is then derived, which is reflected as the error bars in both Figure 3-14(b) and (c). At 6-dB PBO, 36% $\eta_D(\text{PA})$ is achieved, demonstrating $1.36\times/2.72\times$ efficiency enhancement over an idealistic classB/class-A PA.

Alternatively, the TX P_{out} is obtained from the measurement of the PA TS with direct probing. The same PA core used in the TX is implemented as a separate TS with an additional output matching network (OMN) transforming differential 100 Ω to the PA optimum load impedance (R_{opt}/L_{opt}), where R_{opt} is also the antenna input impedance. As shown in Figure 3-14(e), the PA TS achieves 13.6 dBm P_{sat} with 45.4% $\eta_D(\text{PA})$ at 28GHz. The P_{sat} is defined at the 3-dB gain compression point, since the two PAs are driven to the same saturation level during the outphasing operation. Since the PAs directly interface with the antenna in the TX design, realizing on-antenna power combining, the loss from the PA TS OMN should be de-embedded for Pout calculation. A back-to-back OMN TS is also implemented [Figure 3-13(e)] to capture its loss, and the measured S-parameters of the OMN are shown in Figure 3-14(d). At 28 GHz, the passive loss of the back-to-back OMN TS is 1.8 dB, indicating that the passive loss of a single OMN TS is 0.9 dB. After de-embedding the loss from the OMN, the PA achieves 14.5-dBm P_{sat} , with 55.8% $\eta_D(\text{PA})$.

Therefore, considering 3-dB output power increase due to the two-way combining, the P_{sat} based on TS measurement is 17.5 dBm, matching well with the radiation-based P_{sat} value of 17.1 dBm at 28 GHz. The comparison in measured P_{sat} between the radiation-based and probing-based method is also shown in Figure 3-14(b). Overall, the two methods achieve a very close agreement on the measured P_{sat} around 28 GHz. In addition, the radiation-based P_{sat} shows a smaller value at lower frequency range, due to the limited antenna bandwidth [Figure 3-6(c)], compared to a wideband transformer-based OMN [Figure 3-14(d)].

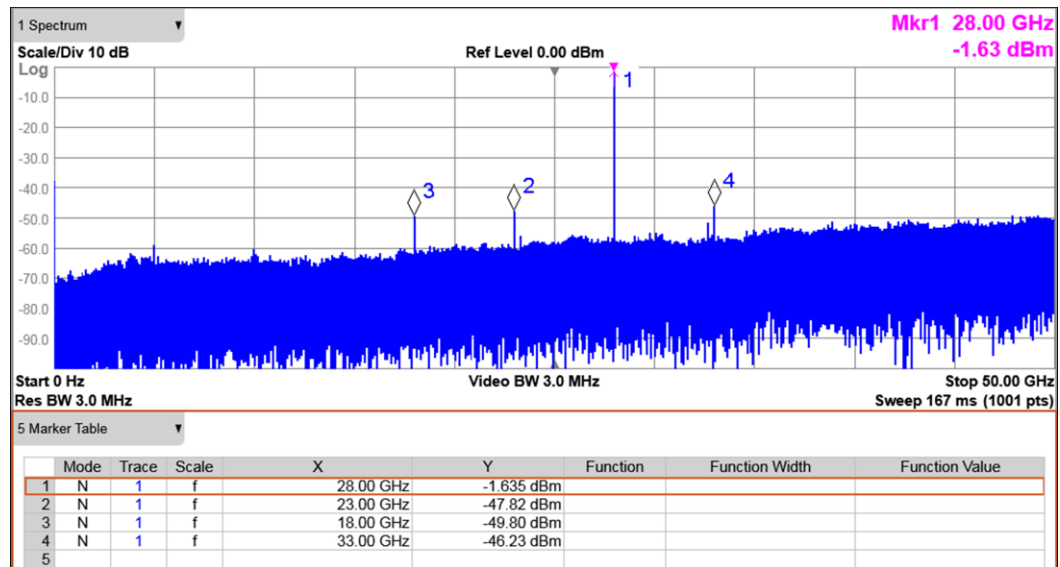


Figure 3-15 Measured TX output spectrum.

The TX output spectrum is measured and shown in Figure 3-15. A horn antenna (SAR-2013-34-S2) and a wideband LNA (RLNA16G32G) are used to receive and amplify the signals before the spectrum analyzer. Except the desired carrier frequency at 28 GHz, the LO leakage (23 GHz), image signal (18 GHz), and IF 2nd harmonic up-conversion (33 GHz) are identified from 18 to 33 GHz. Both the horn antenna and the LNA have around 3-dB gain variation within the same frequency range, which is readily de-embedded for the measurement of the undesirable signal rejection. At least 40-dB rejection is achieved for

the unwanted tones mentioned above, which prevents the corruption of the demodulated signals.

3.3.2 Wireless Modulation Test

To ensure high-performance modulations, the TX large-signal nonlinearities (AM–AM/AM–PM) are first characterized. The measurement setup for AM–AM and AM–PM is shown in Figure 3-16(a). Three channels from AWG are used, with two of them providing the input two-path outphasing signals, and the third channel generating the reference signal for the phase comparison. A signal generator and an external power amplifier (PA) are employed to feed the LO power for both up- and down-conversion. The transmitted signal is picked up by the RX horn antenna and then down-converted to the IF (5 GHz) by the mixer. The IF signal is amplified, sent to the sampling oscilloscope, and compared with the reference IF signal from the AWG for amplitude/phase nonlinearity characterization.

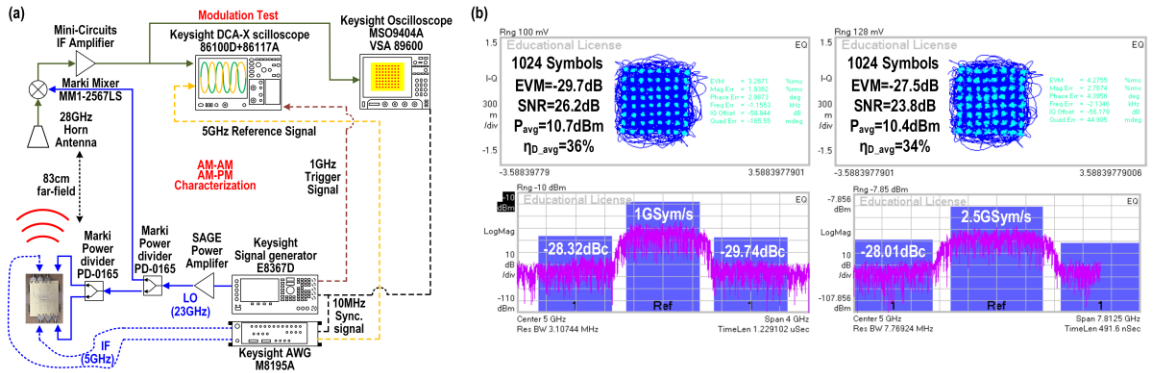


Figure 3-16 (a) Nonlinearity characterization and modulation test setup. (b) Measurement results of 64-QAM at 6 and 15 Gb/s.

By applying the hybrid input conditions (P_{in} , ϕ) shown in Figure 3-12, the measured large-signal behaviors are summarized in Figure 3-14(c). A memoryless 2-D (P_{in} , ϕ) lookup table (LUT) is used to generate the desired outphasing input signals and perform

digital pre-distortion (DPD) to correct the AM–AM/AM–PM errors. Compared with existing outphasing PAs/TXs [31]–[36], no additional computation resource is required.

The wireless modulation measurement setup is shown in Figure 3-16(a). Essentially, the same setup is used only with the sampling oscilloscope replaced by a mixed signal oscilloscope for digital demodulations. As shown in Figure 3-16 (b), the Chireix TX achieves -29.7 -dB EVM with 36% average PA DE (η_{D_avg}) for 6 Gb/s (1Gsym/s) 64-QAM signal, and -27.5 -dB EVM with 34% η_{D_avg} for 15 Gb/s (2.5 Gsym/s) 64-QAM signal, demonstrating state-of-the-art modulation bandwidth and average efficiency. The EVM is referenced to the peak amplitude of the constellation. The TX performance in a wireless testing environment with 64-QAM at different symbol rates is further summarized in Figure 3-17.

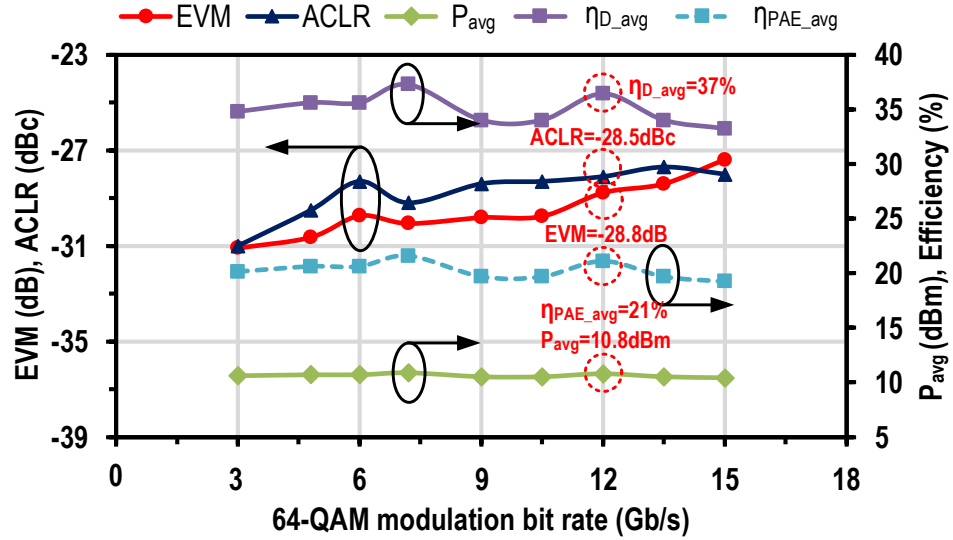


Figure 3-17 Chireix TX modulation performance versus bit rate with 64-QAM.

PA/TX architectures with spatial power combining such as the Spatial IQ Combiner TX [40] and Spatial Outphasing TX [41] are demonstrated in earlier literature. However, these designs exhibit substantially narrower FoV than the intrinsic antenna FoV, due to their vectorial spatial signal combining. Since the desired outphasing or IQ combining only

happens at a specific angle, the signals will be severely distorted when the TX and RX are mis-aligned [40], [41]. Instead, the proposed Chireix TX achieves on-antenna outphasing combining before its radiation and therefore ensures undistorted signals over the full antenna FoV. Figure 3-18 depicts the modulation results of the Chireix TX over various radiation directions. When the receiving angle is swept from -60° to $+60^\circ$, the measured demodulated signals exhibit consistent and angle-independent performance with consistent EVM values over the entire antenna FoV. Such angle-independency is essential for establishing reliable wireless communication links in practical usage scenarios that prefer easy and robust TX/RX alignment. Therefore, our on-antenna outphasing TX is particularly suitable for constructing phased arrays or MIMO systems with wide array scanning angle, which in contrast cannot be achieved by reported Spatial IQ Combiner TX [40] or Spatial Outphasing TX [41] with inherent narrow element FoV.

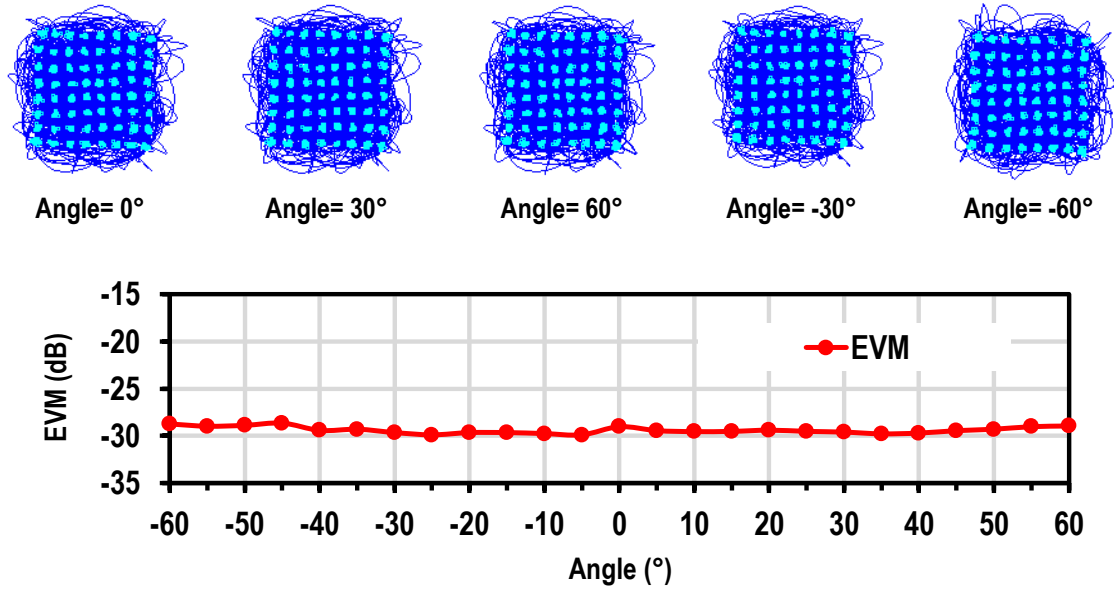


Figure 3-18 Measured modulation results at different directions with 6 Gb/s 64-QAM, demonstrating wide antenna FoV.

3.3.3 PA Reliability Testing

To evaluate the reliability of the CS PA with 1-V supply biasing ($V_{dd} = 1$ V), RF stress testing was performed continuously over a cumulative 24-h period under CW operation. The CS PA TS is used in this test, so that its output power can be directly probed for measurement.

The CS PA chip was driven at the input 1-dB compression point ($IP_{1dB} = -5$ dBm), with P_{out} and PA-stage dc current (I_{DC_PA}) being monitored. The reliability testing results are summarized in Figure 3-19, which reveals that no degradation on the PA performance is observed over continuous 24-h period. In practical applications especially for communication, the PA is mostly used to amplify complex modulated signals with certain PAPR. The average P_{out} during modulation is much less than P_{1dB} (e.g., >6 dB for 64-QAM), which means the RF stress on the PA is largely relaxed in real applications compared to the performed CW reliability testing.

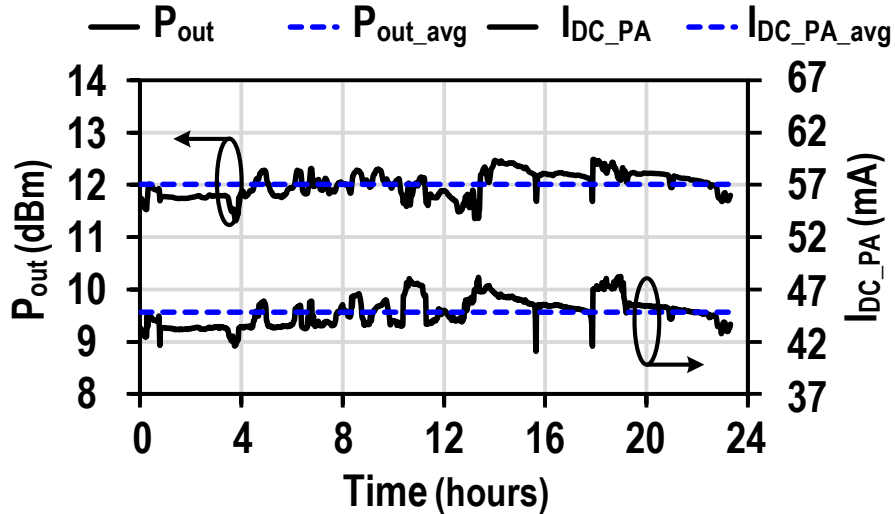


Figure 3-19 PA reliability test at P_{1dB} with P_{out} and I_{DC_PA} being monitored over 24 h ($P_{in} = -5$ dBm, $V_{dd} = 1$ V).

Table 3-1 shows the comparison of the proposed Chireix TX with the state of the art [45]. By exploiting a unique on-antenna outphasing architecture, the Chireix TX demonstrates high-efficiency and high-speed transmission of complex modulated signals

in a wireless testing environment. Measurement proves that the proposed Chireix TX achieves high efficiency both at the peak output power and PBO. Modulation test further shows the TX manages to efficiently transmit up to 15 Gb/s 64-QAM signals in a wireless dynamic environment. In addition, the on-antenna active load modulation network can be implemented with other baseline antennas, such as dipole, patch, spiral antennas. The DLA-based outphasing combiner demonstrated in this paper is only a proof-of-concept example.

Table 3-1 Comparison with state-of-the-art mm-Wave silicon-based PAs/TXs

	This Work	[22] Rabet ISSCC '18	[17] Zhao JSSC '12	[39] Shakib ISSCC '17	[7] Hu ISSCC '17	[40] Park TMTT '16	[41] Ali ISSCC '18	[42] Li ISSCC '18			
Technology	45nm CMOS SOI	130nm SiGe	40nm CMOS	40nm CMOS	130nm SiGe	28nm CMOS	65nm CMOS	130nm SiGe			
Architecture	On-antenna outphasing	Outphasing with on-chip passive	Outphasing with on-chip passive	Analog	Doherty	Analog	Analog with AM-PM correction	Continuous-mode harmonically tuned			
Supply (V)	1.0	4.0	1.0	1.1	1.5	2.2	1.1	1.9			
Frequency (GHz)	28	28	60	27	28	28	28	28.5			
P _{linear} (dBm)	17.1	23	15.6	13.7 (P _{1dB})	15.2 (P _{1dB})	18.6 (P _{1dB})	14 (P _{1dB})	15.2 (P _{1dB})			
η @ P _{linear}	PA	PA	PA	PA + DR	PA	PA + DR	PA	PA+DR	PA	PA+DR	
	53% (DE _{avg}) ± 2.4% (σ) [†]	43% (PAE _{avg}) ± 1.6% (σ) [†]	41.4% (PAE)	25% (PAE)	31.1% (PAE)	28.3% (CE)	19.5% (PAE)	43.3% (PAE)	34.7% (PAE)	43% (PAE)	39.2% (PAE)
η @ 6dB PBO	36% (DE _{avg}) ± 2.1% (σ) [†]	23% (PAE _{avg}) ± 1.5% (σ) [†]	34.7% (PAE)	9% (PAE) [†]	12.5% (PAE) [†]	21% (CE) [†]	11% (PAE) [†]	20% (PAE) [†]	11% (PAE) [†]	19% (PAE) [†]	16% (PAE) [†]
	1.36 (DE)		1.67	0.72	0.8	1.48 (CE)	0.92	0.63	0.88		
Modulation Type and Data Rate	64QAM, 6Gb/s	64QAM, 15Gb/s	64QAM OFDM, 0.48Gb/s	16QAM, 0.5Gb/s	64QAM OFDM with 8CC, 4.8Gb/s	64QAM, 6Gb/s	64QAM WLAN, 0.48Gb/s	64QAM, 2.04Gb/s	64QAM, 18Gb/s		
EVM (dB)	-29.7	-27.5	-30.5**	-22	-25	-26.6	-27.5	-26.4**	-25		
P _{avg} (dBm)	10.7	10.4	14.3	12	6.7	7.2	11.0	9.8	9.8		
η_{avg}	PA	PA	PA	PA	PA + DR	PA	PA	PA+DR	PA+DR		
	$\eta_{\text{DE(PA)}}$	$\eta_{\text{DE(PA)}}$									
	36%	34%									
	PA + DR	PA + DR	$\eta_{\text{PAE(PA)}}$	$\eta_{\text{PAE(PA)}}$	$\eta_{\text{PAE(PA+DR)}}$	$\eta_{\text{CE(PA)}}$	$\eta_{\text{PAE(PA)}}$	$\eta_{\text{PAE(PA+DR)}}$	$\eta_{\text{PAE(PA+DR)}}$		
	$\eta_{\text{PAE(PA+DR)}}$	$\eta_{\text{PAE(PA+DR)}}$	25.3%	15%	11%	14.4%	17.3%	18.2%	18.4%		
	20.6%	19.2%									

[†] Graphically estimated.

^{*} Measurement standard deviation derived from four independent measurements on two different TX modules.

^{*} Compared to an ideal class-B PA with the same efficiency at P_{linear}.

^{**} Referenced to the RMS value of the constellation magnitudes (EVM_{RMS} ≈ SNR) [44].

3.4 Conclusion

This paper presents a Chireix TX architecture that explores multi-feed antennas to achieve unique on-antenna outphasing load modulation and demonstrate high-efficiency transmission of wideband modulated signals. High-efficiency power combining, outphasing load modulation and mm-Wave signal radiation have been realized in a single antenna structure, accomplishing multi-functional signal processing. More importantly, unlike other spatial combining techniques, the proposed Chireix TX preserves a wide

element-level FoV. By leveraging DLA, a proof-of-concept Chireix TX demonstrates measurement performance that advances the state of the art.

CHAPTER 4. A WIDEBAND FREQUENCY DOUBLER WITH TRANSISTOR MULTIPORT WAVEFORM SHAPING FOR 2ND HARMONIC ENHANCEMENT AND 4TH HARMONIC SUPPRESSION

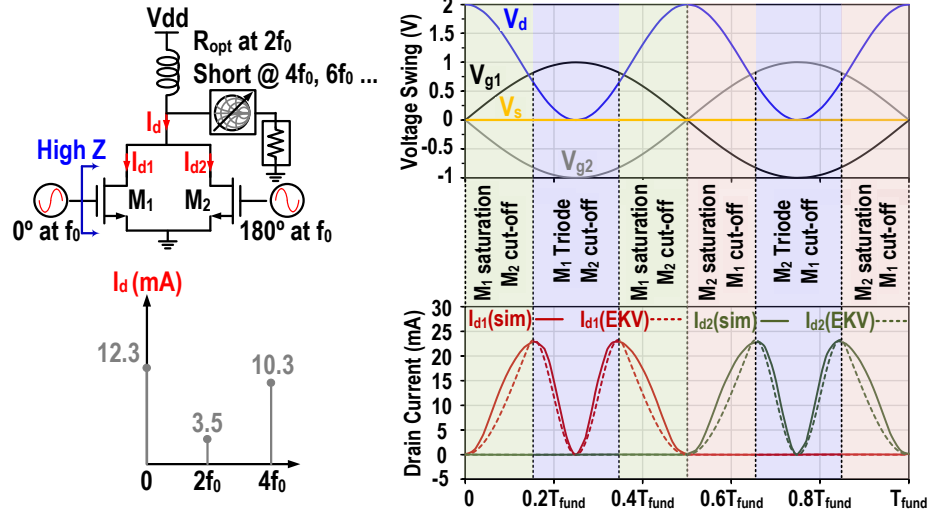
4.1 Introduction

Integrated millimeter-wave (mm-Wave) frontends for communication, radar, and imaging applications demand signal sources with high spectral purity. However, as the operation frequency increases, implementing low phase-noise oscillators becomes exceedingly challenging [46]. Alternatively, a popular solution is to utilize a frequency multiplier that multiplies its lower-frequency input driving signal, for which oscillators and phase-locked loops (PLLs) with high spectral purity can be readily realized on chip. Moreover, input signal distribution at lower frequency introduces less signal loss and amplitude/phase mismatch, particularly suitable for large-scale phased-arrays and MIMO systems [47].

Conventional mm-Wave frequency multipliers suffer from high conversion loss, low DC-to-RF efficiency, limited bandwidth, and output power, which often necessitates a power-hungry output buffer. In this section, we present a frequency doubler topology leveraging transistor multiport waveform shaping to increase the 2nd-order transconductance nonlinearity, suppress the output 4th and odd harmonics, and substantially boost the 2nd harmonic generation efficiency [48]. Moreover, a broadband input 2nd harmonic trap as well as wideband input and output matching networks are implemented on chip to achieve a >60% fractional bandwidth (FBW) from 46 to 89 GHz, making it

favorable for various wideband/multiband mm-Wave applications, such as 5G communication, E-band wireless backhaul, and hyperspectral mm-Wave imaging.

(a) Conventional Topology



(b) Proposed Topology

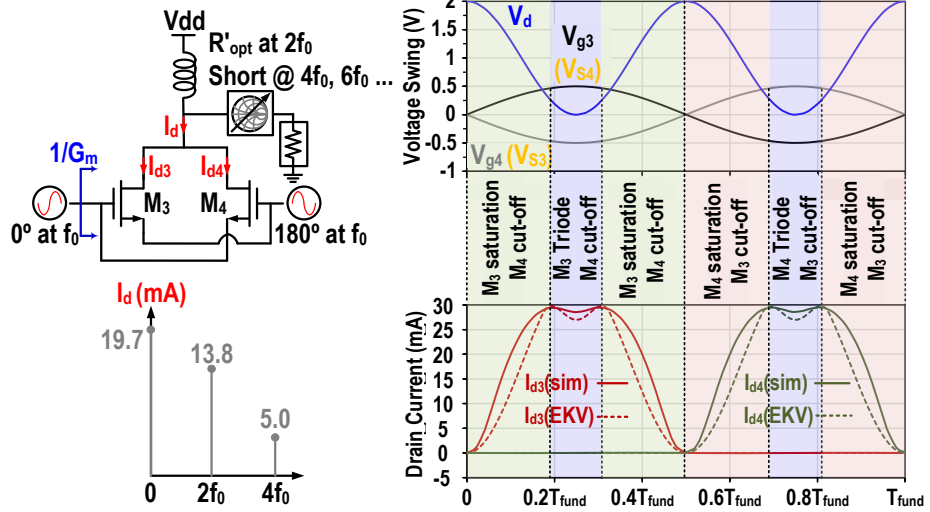


Figure 4-1 Comparison between (a) conventional push–push pair and (b) proposed multiport driven frequency doubler, illustrating current waveform reshaping for 4th harmonic suppression and 2nd harmonic enhancement.

4.2 Theory and Design

A comparison between the conventional push–push pair and the proposed frequency doubler is shown in Figure 4-1. Unlike the conventional doubler with grounded source

terminals, both the gate and source terminals in the proposed doubler are simultaneously driven by 180° out-of-phase signals, whose harmonic waveform shaping advantages will be analyzed later. For a fair comparison, the transistors are biased with 1-V nominal V_{dd} and 0-V gate biasing (Class-C) in both cases. A 1-V input V_{gs} swing is applied to maximize the transistor second-order nonlinearity without sacrificing reliability. Both designs are loaded with their corresponding 2nd harmonic optimum load-pull impedance, leading to rail-to-rail drain voltage swing at $2f_0$ for optimal 2nd harmonic output power and drain efficiency (η_D). A balanced topology guarantees inherent cancellation of f_0 and odd harmonics at the output, only allowing even harmonics to exist. Therefore, high-order ($>2^{\text{nd}}$) even harmonic currents should be minimized to increase the 2nd harmonic power generation efficiency.

In the conventional push–push pair, the transistor M_1 first enters saturation when it is turned on ($V_{g1} > V_{th}$). As a result, M_1 drain current (I_{d1}) starts to increase until $V_{d1} = V_{g1} - V_{th}$, after which M_1 enters triode region. The further rising gate voltage drives M_1 into deep triode, resulting in a large bifurcation in its current waveform [Figure 4-1(a)]. M_1 later goes back to saturation with decreasing V_{g1} , and I_{d1} starts falling. Adding I_{d1} and I_{d2} together, the total drain current I_d waveform consists of a strong undesired 4th harmonic, resulting in reduced 2nd harmonic current. This is further verified by its simulated spectrum [Figure 4-1 (a)].

To suppress the wasted 4th harmonic current, transistor multiport excitations are exploited to reshape the output current waveform for enhancing the 2nd harmonic current generation. In the proposed doubler, the same 1-V V_{gs} swing is maintained to drive the device into large-signal nonlinear regime. However, due to the source driving, the gate voltage swing (V_{g1} and V_{g2}) is directly reduced by half, which shortens the transistor triode period and greatly reduces the drain current bifurcation, as shown in the simulated current waveform (I_{d3} and I_{d4}) and spectrum [Figure 4-1(b)]. The EKV FET model [49], [50] is

used to mathematically analyze the current waveform shaping in both conventional and proposed structures, which agrees well with the circuit simulations (Figure 4-1). In addition, compared to the high input impedance in the conventional push–push pair, the input impedance is lowered to $1/G_m$ in the proposed structure. This greatly eases the doubler input impedance matching to the $50\ \Omega$ interface for broadband mm-Wave operation.

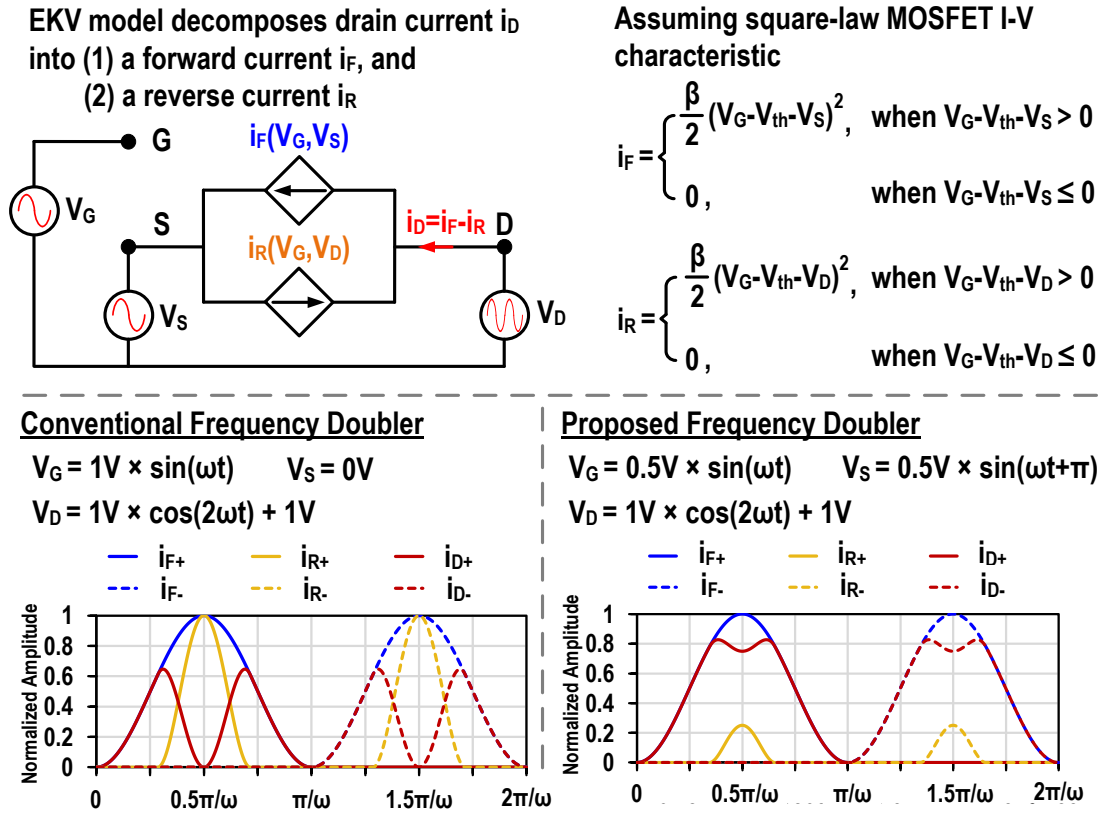


Figure 4-2 EKV FET model used to mathematically analyze the current waveform in the conventional and proposed frequency doubler structures.

As shown in Figure 4-2, the EKV FET model decomposes transistor drain current i_D into a forward current i_F (from drain to source) and a reverse current i_R (from source to drain), which is governed by transistor terminal voltage swings. The EKV model is known for its accurate and continuous modeling FET characteristics, including strong to weak inversion and triode regions. Thus, it is adopted to analyze the current waveforms in both

the conventional and proposed frequency doublers, showing 4th harmonic suppression and 2nd harmonic enhancement of the drain current i_D in the proposed scheme, agreeing well with the transistor circuit simulations shown in Figure 4-1.

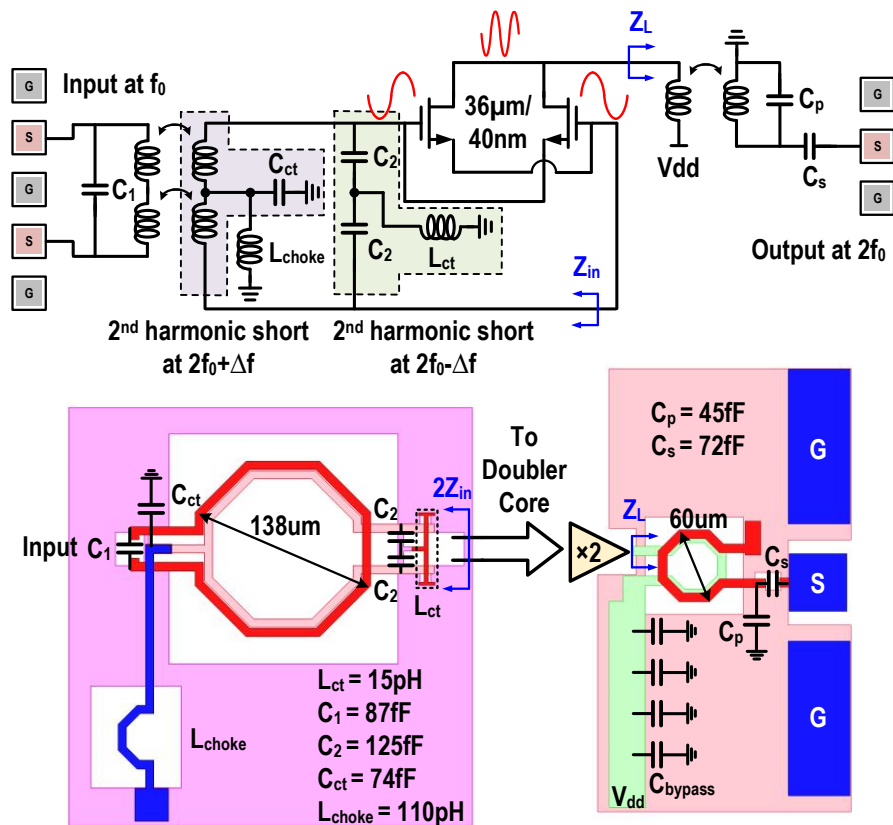


Figure 4-3 Top-level multiport driven frequency doubler schematic with wideband dual-resonance input 2nd harmonic trap filter and the corresponding passive structures.

The top-level circuit schematic and the corresponding passive structures are shown in Figure 4-3. Wideband input matching at f_0 and wideband input 2nd harmonic trap are realized in a compact footprint. Without the 2nd harmonic trap, the $2f_0$ voltage swing appears at the gate terminals by C_{gd} feedback, generating undesired 180° out-of-phase $2f_0$ drain current and canceling the desired $2f_0$ output current. Thus, trapping the 2nd harmonic at the input is necessary over the entire doubler bandwidth. A dual-resonance 2nd harmonic trap filter is created to provide short termination for 2nd harmonic at the input. Shown in

Figure 4-3, C_{ct} is used to resonate out the transformer common-mode inductance, resulting in the first 2nd harmonic short at $2f_0 + \Delta f$. L_{ct} forms another series resonance with C_2 (used for input matching at f_0 as well), leading to the second trap at $2f_0 - \Delta f$. By offsetting the two resonant frequencies, a wideband input 2nd harmonic trap is therefore created. Note that the center taps of the transformer and the two capacitors (C_2) are virtually grounded in the differential mode at f_0 , so neither C_{ct} nor L_{ct} affects the fundamental impedance matching, which decouples the impedance tuning at f_0 and $2f_0$. At the doubler output, another wideband transformer balun is employed, converting 50 Ω to the 2nd harmonic optimum load-pull impedance.

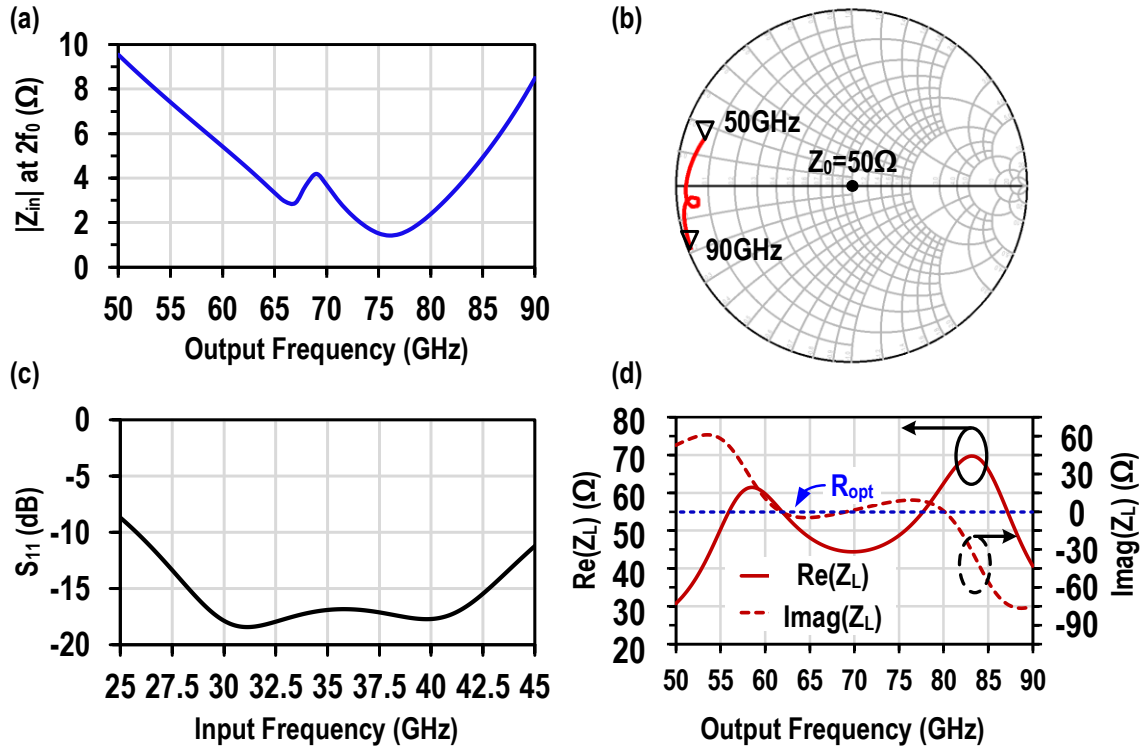


Figure 4-4 Simulation results of the (a) wideband input second-order harmonic trap and (b) its trajectory on Smith Chart, (c) broadband input matching, and (d) impedance seen by the doubler core (Z_L) at the output.

The simulation results of the wideband input/output matching and 2nd harmonic trap are summarized in Figure 4-4. It clearly shows that two resonances offset in frequency

are formed to extend the bandwidth of the 2nd harmonic input low impedance [Figure 4-4 (a)], which is further verified by its trajectory on the Smith Chart [Figure 4-4 (b)]. Due to the reduced input impedance in the proposed doubler, a wideband input matching at f_0 is also realized with S_{11} below -10 dB from 25 GHz to over 45 GHz [Figure 4-4 (c)]. The achieved 2nd harmonic real/imaginary load impedance Z_L seen by the doubler output after absorbing the device output capacitances is also plotted together with the optimum load-line impedance R_{opt} [Figure 4-4 (d)]. A close matching is achieved over a large frequency range, enabling wideband maximum 2nd harmonic power extraction.

4.3 Measurement Results

The wideband high-efficiency frequency doubler is implemented in a 45-nm CMOS-silicon-on-insulator (SOI) process (Figure 4-5). Excluding pads, the core area only occupies $370\ \mu\text{m}$ by $270\ \mu\text{m}$, allowing for its compact integration in mm-Wave transceiver frontend systems.

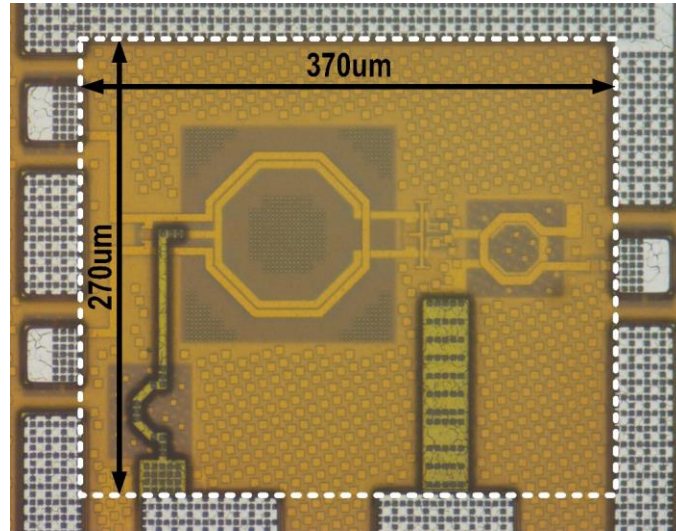


Figure 4-5 Die micrograph (core area: $370\ \mu\text{m} \times 270\ \mu\text{m}$).

The measured doubler output power (P_{out}) and conversion gain (CG) under different supply biasing ($V_{dd} = 1.1, 1.0$, and 0.9 V) are summarized in Figure 4-6. With

fixed input power ($P_{in} = 11$ dBm), the P_{out} is kept within 3-dB variation from 46 to 89 GHz [Figure 4-6(a)], achieving >60% instantaneous FBW without any tuning or band-switching elements. The saturated power (P_{sat}) is also measured [Figure 4-6(b)], showing a peak value of 7.4 dBm without using any output buffer and achieving a flat frequency response with a 51% 1-dB P_{sat} FBW covering from 50 to 84 GHz. Figure 4-7 depicts the large-signal behaviors of the frequency doubler at the output frequency of 60 GHz, showing a P_{sat} value of 7 dBm.

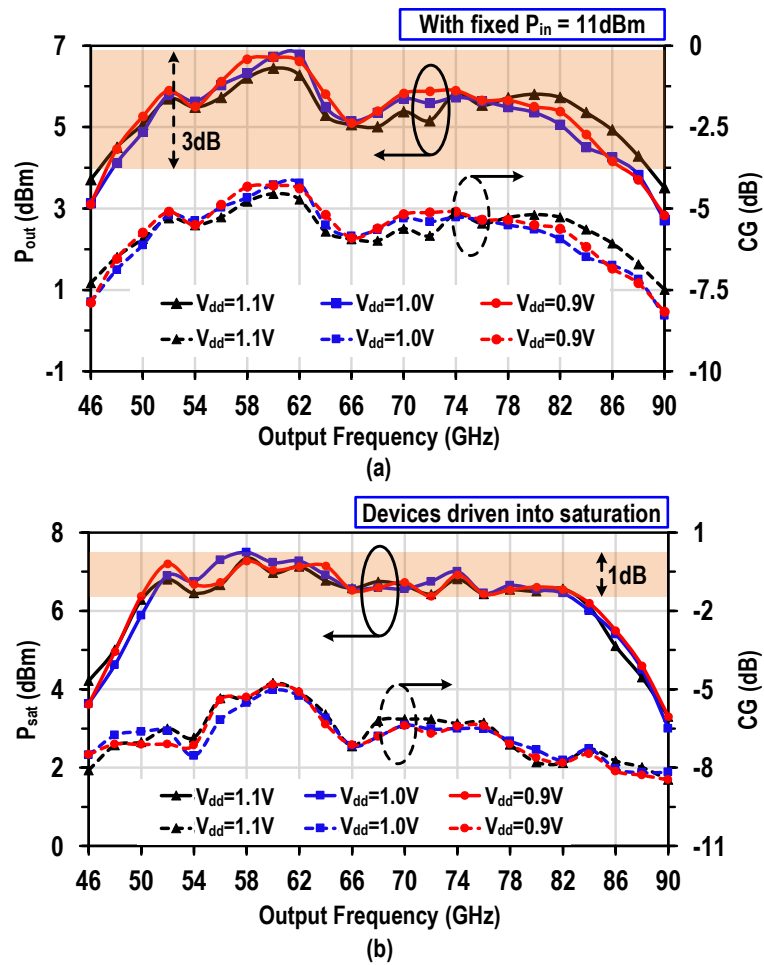


Figure 4-6 Measured P_{out} and CG of the multipoint driven frequency doubler (a) with fixed P_{in} and (b) at saturation.

Shown in Figure 4-8, a maximum η_D of 25% is achieved at 60 GHz with 0.9-V dc supply, while at least 15% η_D is obtained from 49 to 87 GHz. The phase noise before (25

GHz) and after (50 GHz) the frequency doubling is measured and plotted in Figure 4-9. The power delivered to the spectrum analyzer is maintained to be the same when measuring the phase noise of the input and output signal. In theory, the phase-noise degradation due to frequency multiplication ($\times N$) is given by $20 \times \log(N)$. A 6 dB increase in phase noise is observed in measurement, verifying no additional phase noise or spurious tone from the proposed multiport driven doubler.

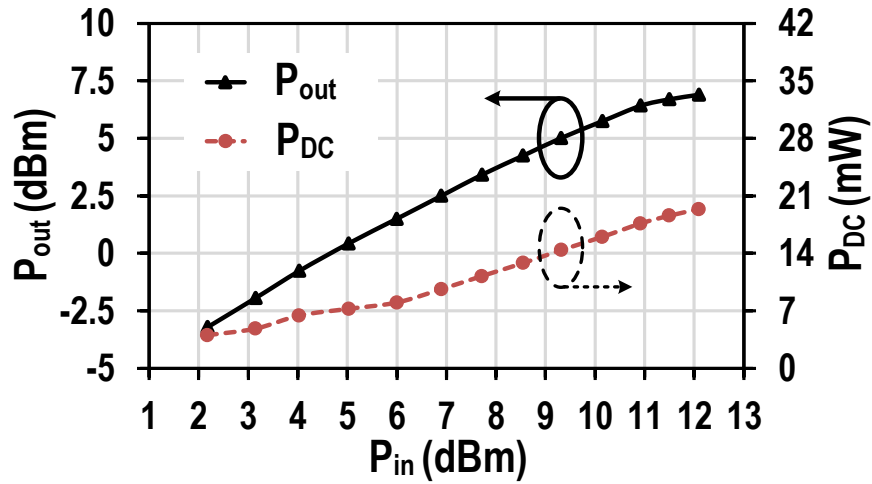


Figure 4-7 Measured frequency doubler output power and dc power consumption versus input power at the output frequency of 60 GHz.

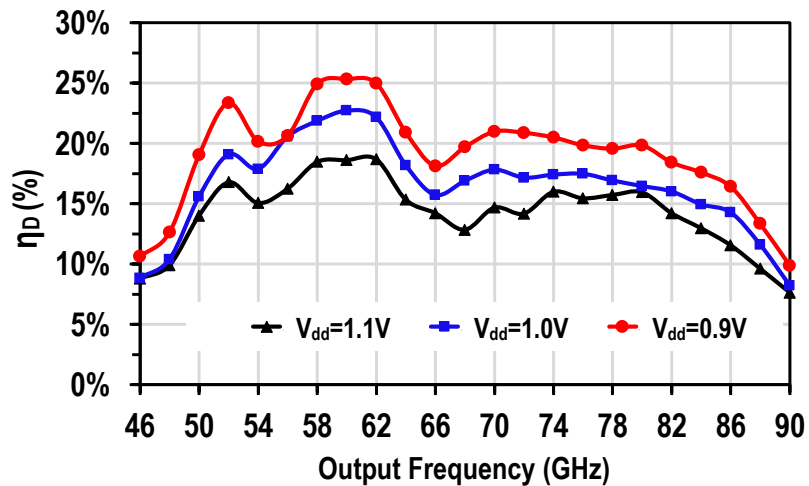


Figure 4-8 Measured drain efficiency η_D of the multiport driven frequency doubler over frequencies.

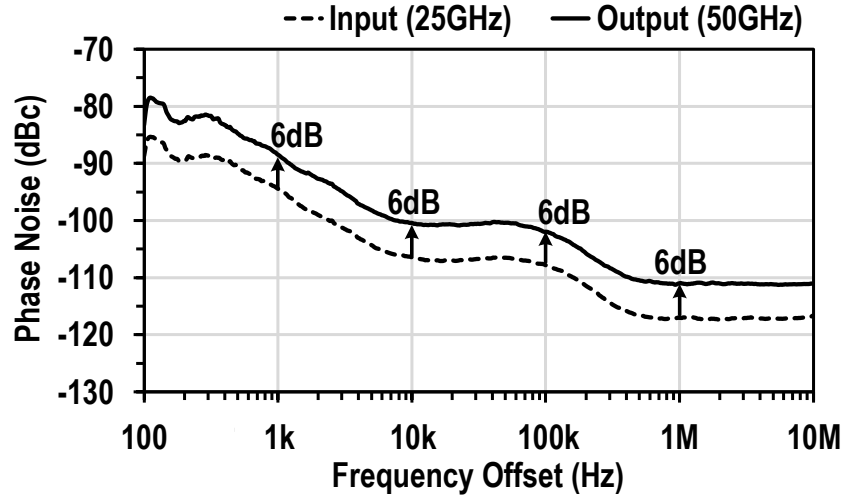


Figure 4-9 Measured averaged phase noise before (at 25-GHz input) and after (at 50-GHz output) the frequency doubling.

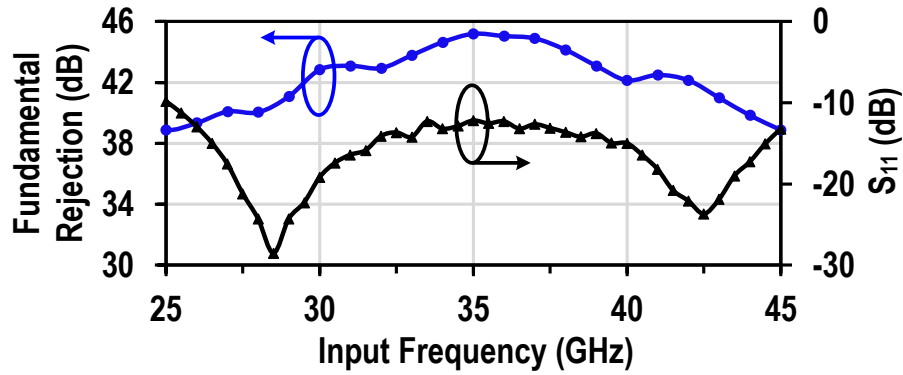


Figure 4-10 Measured fundamental signal rejection and large-signal S_{11} of the multiport driven frequency doubler.

The doubler fundamental frequency rejection is measured at P_{sat} across the frequencies (Figure 4-10). At least 38-dB fundamental rejection is achieved over the doubler operation bandwidth. The large-signal input matching shows a -10 dB S_{11} bandwidth from 25 to 45 GHz (Figure 4-10). The output spectrum is also captured in measurement, as shown in Figure 4-11. The inconsistency of noise floor is due to the switch between different harmonic mixing or change in mixing LO at band crossings for the internal receivers in the 110-GHz Keysight N9041B UXA signal analyzer. After calibrating the cable loss at 30, 60, and 90 GHz, the fundamental signal rejection is 43.1

dB and the 3rd harmonic rejection is 42.2 dB. Compared with the reported mm-Wave frequency doublers at similar frequencies (Table 4-1), this work achieves the highest doubler core efficiency (even including designs with output buffers). It also achieves the largest instantaneous operation bandwidth without any tuning or band-switching elements.

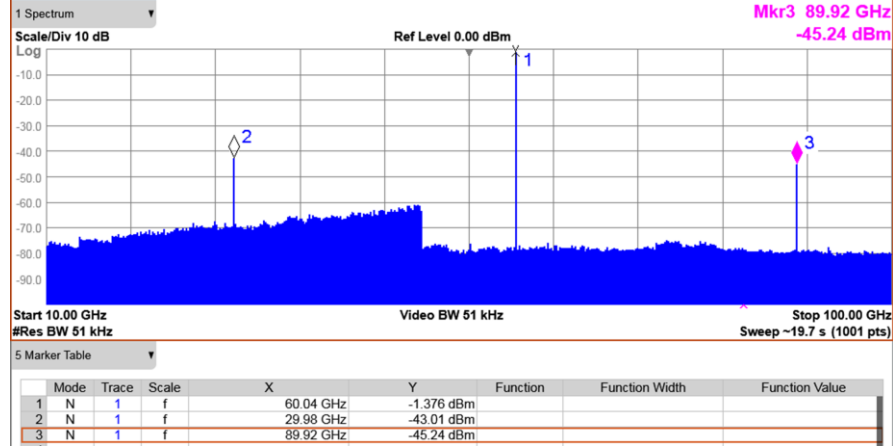


Figure 4-11 Measured output spectrum of the multiport driven frequency doubler.

Table 4-1 Comparison with State-of-the-art mm-Wave Frequency Doublers

	This Work	[7]	[8]	[9]	[10]
Technology	45nm CMOS SOI	65nm CMOS	65nm CMOS	90nm SiGe	0.1μm GaAs pHEMT
Topology	Transistor multi-port waveform shaping	Conventional push-push pair	Injection-locked frequency doubler	Kimura doubler with active load using CMFB	Traveling-wave frequency doubler
Output Buffer [†] (Y/N)	N	N	Y (2-stage CS Buffer)	Y (Cascode Buffer)	N
3dB Bandwidth	46-89GHz* (64% FBW)	62-90GHz (37% FBW)	77-87GHz [†] (12% FBW)	10-50GHz ^{†,°} (133% FBW)	85-110GHz (26% FBW)
Peak η_D	25% (>15%, 49-87GHz)	11.5%**	2.2%**	<0.3%**	14%**
Peak η_{total} = $P_{out}/(P_{DC}+P_{in})$	15.5% (>10%, 50-85GHz)	9.7% (>6%, 62-78GHz)	1.8%**	<0.3%**	11.2%
P_{sat} (dBm)	7.4	2.5	-5.96	-2 [†] (at 10GHz)	9
Peak CG (dB)	-4.3	-2.5	-9.36**	12 (at 10GHz)	3.2
Fundamental Rejection (dB)	>38	>20	N.A.	>22	>30
P_{DC} (mW)	17-20	9-14	9.7-11.4	250	45-56

[†] Graphically estimated.

[‡] An implementation with output buffer increases the overall frequency doubler efficiency.

* Instantaneous bandwidth with fixed input power.

** Calculated based on reported values.

° With tunable load.

4.4 Conclusion

The transistor multiport waveform shaping is proposed in this letter to boost the 2nd harmonic generation in the frequency doubler. As a result, the doubler efficiency is significantly improved as compared to the conventional push–push pair. The EKV FET model is used to theoretically analyze the current waveform behaviors in both the conventional and proposed structures, which agrees well with the circuit schematic simulation results. Wideband frequency doubling performance is achieved by the broadband fundamental matching and the dual-resonance 2nd harmonic trap filter. Implemented in a 45-nm CMOS-SOI process, the multiport driven frequency doubler demonstrates 25% peak drain efficiency, instantaneously covering a 3-dB bandwidth of 46–89 GHz (64% FBW) without using any tuning or band-switching element.

CHAPTER 5. A MM-WAVE CURRENT-MODE INVERSE OUTPHASING TRANSMITTER FRONT-END: A CIRCUIT DUALITY OF CONVENTIONAL VOLTAGE-MODE OUTPHASING

5.1 Introduction

Millimeter-wave (mm-wave) offers broader spectra and proportionate increases of channel capacity. As a result, it is envisioned that 5G-and-beyond communication systems will extensively employ mm-wave spectra to address the exponentially growing data-rate demand. Viable mm-wave transmitter (TX) front-end solutions are expected to support multi-gigabit per second spectrum-efficient modulated signals, such as high-order quadrature amplitude modulations (QAMs) [51], [52]. Moreover, to mitigate the potential severe channel conditions (e.g. selective fading, interference, and multipath effects) when transmitting wideband signals, Orthogonal Frequency Division Multiplexing (OFDM) is widely employed in latest high data-rate wireless communication systems. The corresponding large peak-to-average power ratios (PAPRs) of the high-order QAM and OFDM push the already stringent linearity-efficiency requirements on the deployed TXs/power amplifiers (PAs) [53], [54]. On one hand, the TX/PA must exhibit excellent linearity over a large dynamic range to maintain the signal fidelity. On the other hand, the TX/PA should enhance its efficiency at power back-off (PBO) to minimize overall power consumption and alleviate thermal management. Such demands have stimulated extensive research on new TX/PA architectures to further advance the performance envelope at mm-wave [55]-[60].

Among various TX/PA architectures with PBO efficiency improvement, Doherty TX/PA is possibly the most popular technique at mm-wave. However, it faces several fundamental challenges at mm-wave. Due to inefficient Doherty combiners and imperfect

Main/Auxiliary interactions, many mm-wave Doherty TXs/PAs exhibit either compromised efficiency at peak P_{out} , or low efficiency enhancement at PBO. To address these challenges, adaptive bias circuits or a digitally controlled auxiliary path is employed to achieve rapid ramp-up of the auxiliary PA, which however leads to limited modulation speed. Moreover, the necessary Doherty impedance inverters, i.e., $\lambda/4$ transmission line or its equivalence, further limits the operation bandwidth.

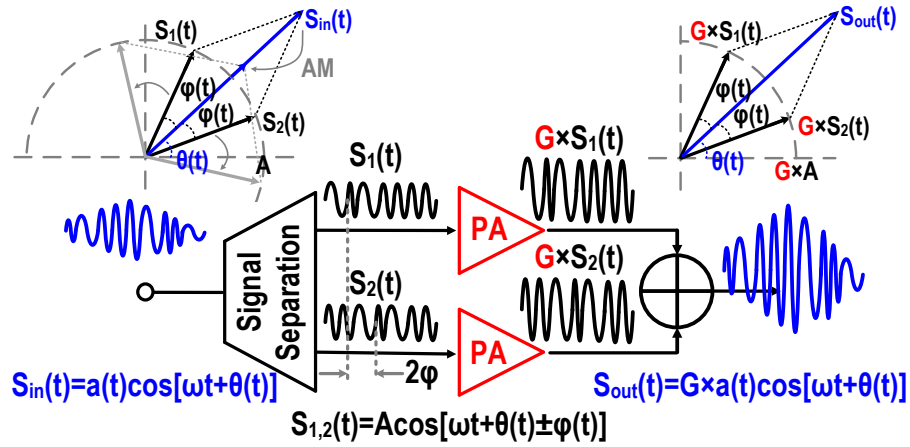


Figure 5-1 Outphasing architecture and its vector representation.

Alternatively, outphasing can achieve improved PBO efficiency while maintaining a high peak efficiency. A typical outphasing architecture consists of two TX/PA branches that operate with their saturated voltage swings but dynamically varying phase difference to synthesize the desired amplitude modulation of the signals (Figure 5-1). Due to the saturated device operation, outphasing TXs/PAs push the P_{out} range towards the saturated output power (P_{sat}), and thus maximize the peak efficiency. Moreover, the outphasing active load modulation enables further efficiency enhancement at PBO. The rapid advance in baseband processors in deeply scaled CMOS reduces the necessary digital computation power for outphasing signal generation. Recent research effort has also focused on a single RF input approach for outphasing signal generation, eliminating the outphasing modulator

[61]-[65]. Consequently, outphasing remains an attractive technique for mm-wave TXs/PAs in future communication systems.

This chapter is organized as follows. Section 5.2 discusses the conventional outphasing topology and its limitations especially at mm-wave. Section 5.3 presents the proposed current-mode inverse outphasing architecture, and a proof-of-concept implementation of the 28GHz TX front-end. The experimental results are summarized in Section 5.4. Section 5.5 finally concludes this chapter.

5.2 Conventional Voltage-Mode Outphasing Architecture and Its Limitations at Mm-Wave

As shown in Figure 5-1, an outphasing system decomposes a complex modulation signal $S_{in}(t) = a(t)\cos[\omega t + \theta(t)]$ into two constant envelope/amplitude components $S_{1,2}(t) = A\cos[\omega t + \theta(t) \pm \varphi(t)]$, whose vector sum is $S_{in}(t)$. Therefore, the amplitude modulation (AM) of the input signal is encoded in the real-time outphasing angle φ between S_1 and S_2 . Theoretically, the constant amplitude A and outphasing angle φ should follow the relationships below as

$$A = \max \left[\frac{a(t)}{2} \right], \quad (5-1)$$

$$\varphi(t) = \cos^{-1} \left[\frac{a(t)}{2A} \right]. \quad (5-2)$$

The outphasing active load modulation is facilitated by two voltage sources driving a non-isolating series power combiner, which serves as the fundamental requirements for the conventional outphasing architecture. Figure 5-2a depicts the conventional voltage-mode outphasing structure with a transformer-based series power combiner. Alternatively, a non-

isolating network with $\lambda/4$ transmission lines can also work as an outphasing combiner [60]. In Figure 5-2a, when driven by two outphased voltage sources ($Ve^{j\varphi}$ and $Ve^{-j\varphi}$), the output network carries a current with a value of

$$I = \frac{Ve^{j\varphi} + Ve^{-j\varphi}}{R_L} = \frac{2V}{R_L} \cos(\varphi). \quad (5-3)$$

The resulting output power (P_L) can be expressed as

$$P_L = \frac{1}{2} I^2 R_L = \frac{2V^2}{R_L} \cos^2(\varphi). \quad (5-4)$$

To obtain the load impedances seen by each PA, the Y-parameters (before adding the Chireix compensation) looking into the output network are first derived as

$$Y_{\pm\varphi} = \frac{I}{Ve^{\pm\varphi}} = \frac{2}{R_L} [\cos^2(\varphi) \mp j \frac{1}{2} \sin(2\varphi)]. \quad (5-5)$$

From (5-5), we observe that the parallel load resistance (R_p) is actively modulated by the outphasing angle φ following

$$R_p = \frac{1}{\text{Re}(Y_{\pm\varphi})} = \frac{R_L}{2\cos^2(\varphi)}. \quad (5-6)$$

The normalized P_L and load resistance R_p versus outphasing angle φ are plotted in Figure 5-2b, illustrating the outphasing active load modulation (e.g. $R_p = 4R_L$ at 6dB PBO when $\varphi = 60^\circ$). In addition, there is a parallel reactive component at each PA output intrinsically associated with the outphasing operation. The phase leading path $S_1(t)$ observes an inductive load, as

$$R_p = \frac{1}{\text{Re}(Y_{\pm\varphi})} = \frac{R_L}{2\cos^2(\varphi)}. \quad (5-7)$$

while the phase lagging path $S_2(t)$ sees a capacitive load, as

$$C_p = \frac{\text{Im}(Y_{-\varphi})}{\omega} = \frac{\sin(2\varphi)}{\omega \times R_L}. \quad (5-8)$$

It should be noted that the use of saturated linear PAs (such as Class-B) cannot cope with such power dependent reactive load impedances, leading to substantial PBO efficiency degradation. Thus, Chireix compensations are required to cancel out the reactive loads at a predefined compensation angle φ_c for better PBO efficiency enhancement. In the conventional case (Figure 5-2a), parallel Chireix compensations $C_p(\varphi_c)$ and $L_p(\varphi_c)$ are thus added for the susceptance cancellation.

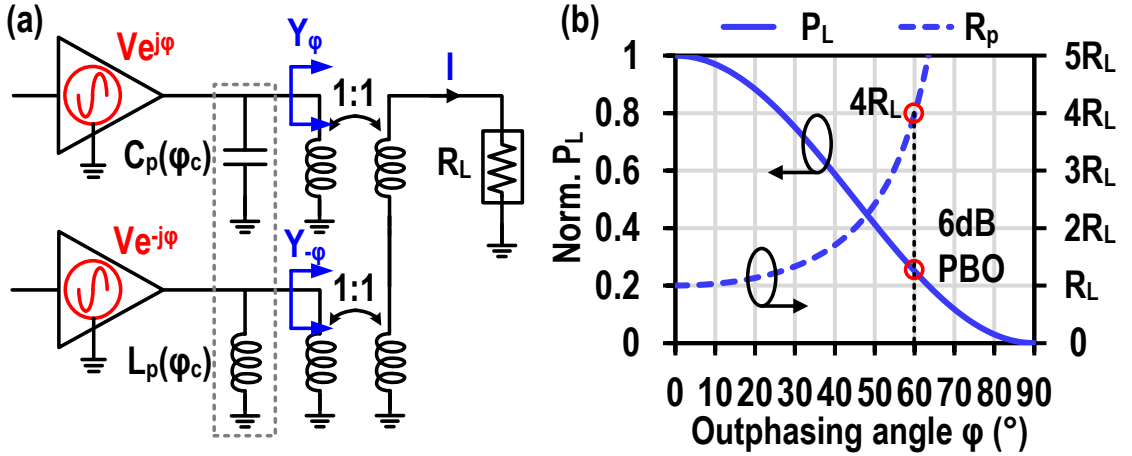


Figure 5-2 (a) Conventional voltage-mode outphasing architecture with a series power combiner. (b) Theoretical outphasing active load modulation.

At mm-wave, the required voltage-mode driving sources and the series output power combiner are the two major limitations on the use of conventional voltage-mode outphasing architecture. First, there is a lack of mm-wave series power combiners for low-

loss voltage-mode outphasing load modulation. Recently, the on-antenna outphasing [37] and triaxial-balun-based outphasing [36] have been demonstrated at 28GHz, as two examples of mm-wave non-isolating outphasing series power combiners. Secondly, the conventional outphasing architecture requires two voltage-mode PAs with low output impedance. At mm-wave, they are approximated by overdriven Class-B common-source (CS) PAs [65], [66], since standard voltage-mode PAs (e.g., Class-D PAs) become very inefficient at mm-wave. This however results in limited achievable P_{out} , linearity, and power-added efficiency (PAE) at PBO. In addition, overdriven CS PAs largely sacrifice the device power gain, which limits the use of conventional outphasing for high mm-wave applications, where device gain is often limited and affects the PA energy efficiency directly.

To further the theoretical understanding on how non-ideal voltage-sources (e.g. overdriven PA approximation) will affect the conventional outphasing performance, we consider a voltage driving source with nonzero output impedance (Figure 5-3a). For simplicity, this analysis uses a real output impedance. The PA output voltages ($V_{\pm\varphi}$) are thus changed to

$$V_{\pm\varphi} = Ve^{\pm j\varphi} - IR_{\pm\varphi}, \quad (5-9)$$

where $R_{\pm\varphi}$ represents the output resistance of the voltage-mode PAs. The series output network performs voltage combining, which leads to

$$V_L = V_{\varphi} + V_{-\varphi} = IR_L, \quad (5-10)$$

where V_L is the voltage on the output load. From (5-9) and (5-10), the load voltage can be solved as

$$V_L = 2V \cos(\varphi) \frac{R_L}{R_L + 2R_o}, \quad (5-11)$$

assuming $R_\varphi = R_{-\varphi} = R_o$, and the output power can therefore be obtained as

$$P_L = \frac{2V^2}{R_L} \cos^2(\varphi) \frac{R_L^2}{(R_L + 2R_o)^2}. \quad (5-12)$$

Comparing (5-12) with (5-4), we can observe that the output power and efficiency drop as a result of the ohmic loss from the output resistance R_o , with a loss factor of $\sigma_1 = \frac{R_L^2}{(R_L + 2R_o)^2}$.

For voltage-mode PAs like Class-D, the output resistances ($R_{\pm\varphi}$) is composed of the PMOS pull-up resistance (R_{oP}) and NMOS pull-down resistance (R_{oN}). Its fundamental component contributes to a constant loss factor $\sigma_2 = \frac{R_L^2}{(R_L + R_{oP} + R_{oN})^2}$ [35]. Therefore, neither the efficiency at PBO nor the linearity (φ -AM) will be affected. When implemented with saturated linear PAs (e.g. overdriven Class-B PAs), the voltage-mode outphasing architecture commonly employs decreasing input driving strength with a limited outphasing angle (e.g. $\varphi \leq 60^\circ$) at PBO for a better PAE, linearity, and dynamic range [36], [38], [60]. However, the output resistance of linear PAs changes dramatically versus the output power. A common-source (CS) and cascode Class-B PA are simulated with their power gain (G_{CS} and G_{Cas}) and output resistances ($R_{o_{CS}}$ and $R_{o_{Cas}}$) plotted in Figure 5-3b.

First, $R_{o_{CS}}$ and $R_{o_{Cas}}$ decrease noticeably after the devices are deeply compressed, which explains why an overdriven linear PA, especially the CS PA, can be approximated as a voltage-mode source and thus used in mm-wave voltage-mode outphasing architecture. Secondly, the increased R_o at PBO will not only lead to a reduced efficiency at PBO, but also cause major φ -to-AM and AM-AM distortions. Last but not the least, the

gain compression in the voltage-mode outphasing operation directly impacts the energy efficiency.

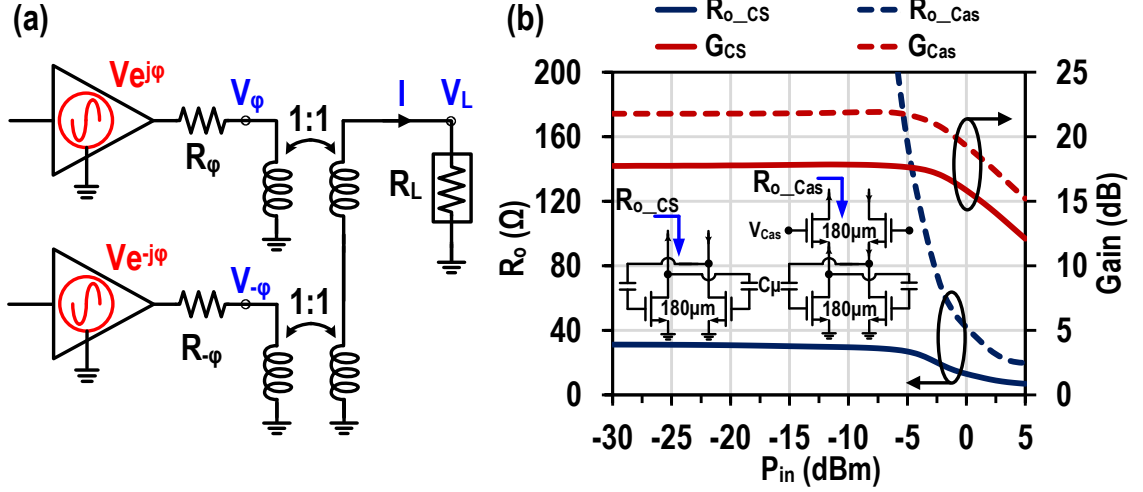


Figure 5-3 (a) Conventional voltage-mode outphasing with nonzero output resistance. (b) Simulated power gain and output resistance of a CS and cascode PA core at 28GHz.

Moreover, if we take the Chireix compensation into consideration (Figure 5-4a), the PA output voltage $V_{\pm\varphi}$ can be determined from

$$V e^{j\varphi} - V_\varphi = \left(\frac{V_\varphi}{Z_C} + \frac{V_L}{R_L} \right) R_o, \text{ and} \quad (5-13)$$

$$V e^{-j\varphi} - V_{-\varphi} = \left(\frac{V_{-\varphi}}{Z_L} + \frac{V_L}{R_L} \right) R_o, \quad (5-14)$$

where Z_C and Z_L are the impedances of the capacitive and inductive Chireix compensation from (5-7) and (5-8) for a predefined compensation angle φ_c . Due to the symmetry of the outphasing operation, we notice that

$$\frac{1}{Z_C} + \frac{1}{Z_L} = 0. \quad (5-15)$$

From (5-13)-(5-15) and (5-10), the load voltage V_L can be solved as

$$V_L = \frac{2V[\cos(\varphi) + \frac{R_o}{R_L} \sin(2\varphi_c) \sin(\varphi)]}{1 + \frac{2R_o}{R_L} + \frac{R_o^2}{R_L^2} \sin^2(2\varphi_c)}. \quad (5-16)$$

Comparing (5-16) with the ideal outphasing relationship $V_L = 2V \cos(\varphi)$, the use of Chireix compensation further introduces an undesired dependence of V_L on the outphasing angle φ . To illustrate such dependence, equation (5-16) is plotted in Figure 5-4b with overdriven CS Class-B PAs. The PAs operate at 3dB compression point with $R_o = 10\Omega$ (Figure 5-3b), $V = 1V$, $R_L = 50\Omega$, and φ_c is chosen as 30° . From Figure 5-4b, we find that the nonzero source resistance clearly results in a reduced V_L . More importantly, the peak amplitude now happens at a shifted outphasing angle φ_o . φ_o can be simply obtained by evaluating the derivative of (5-16), which leads to

$$\varphi_o = \tan^{-1} \left[\frac{R_o}{R_L} \sin(2\varphi_c) \right]. \quad (5-17)$$

As a result, the relationships described by (5-16) and (5-17) should be used for AM-to- φ conversion and outphasing signal generation to avoid the linearity distortion caused by the introduction of Chireix compensation.

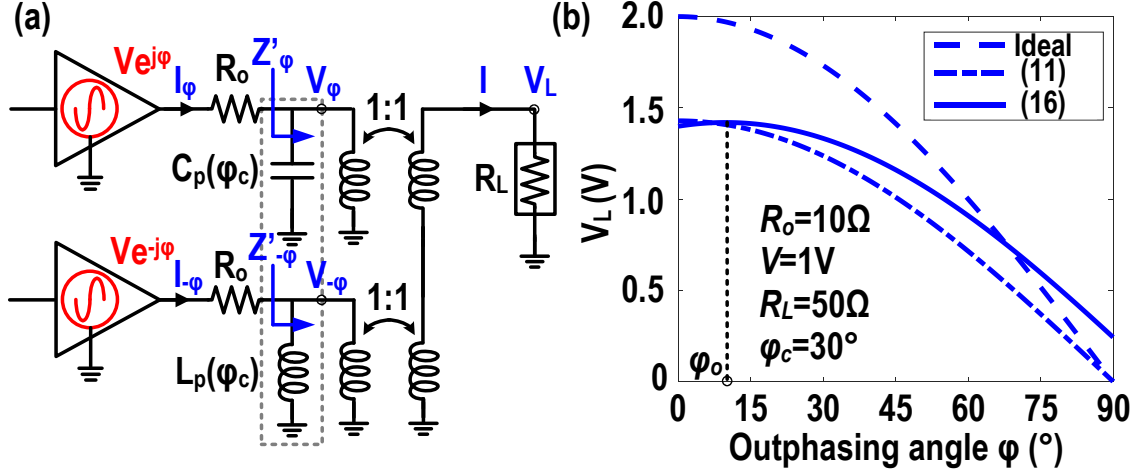


Figure 5-4 (a) Conventional voltage-mode outphasing with nonzero output resistance and Chireix compensation. (b) Theoretical ϕ - V_L relationship in ideal outphasing, and practical cases depicted by (11) and (16).

To evaluate the impact of R_o on the theoretically achievable efficiency by the conventional outphasing architecture, we assume an ideal Class-B PA operation. Therefore, its DC current I_{DC} is related to its fundamental current ($I_{\pm\phi}$) amplitude in a relationship of $I_{DC} = \frac{2}{\pi} |I_{\pm\phi}|$. $I_{\pm\phi}$ can be derived from

$$\phi_o = \tan^{-1} \left[\frac{R_o}{R_L} \sin(2\phi_c) \right]. \quad (5-18)$$

From (5-5), the impedances looking into the Chireix combiner ($Z'_{\pm\phi}$) can be obtained as

$$Z'_{\pm\phi} = \frac{1}{Y'_{\pm\phi}} = \frac{R_L}{2\cos^2(\phi) \mp j[\sin(2\phi) - \sin(2\phi_c)]}. \quad (5-19)$$

As a result, the outphasing efficiency (η_{op}) is given by

$$\eta_{op} = \frac{P_L}{P_{DC}} = \frac{\frac{V_L^2}{2R_L}}{2V_{DD}I_{DC}} = \frac{\pi V_L^2}{8V|I_{\pm\varphi}|R_L}, \quad (5-20)$$

where V_{DD} is the PA DC supply voltage. Combining (5-16) and (5-18)-(5-20), η_{op} can be solved with a closed-form solution, and its dependence on R_o is plotted in Figure 5-5. The Chireix compensation angle φ_c is kept at 30° , while the outphasing angle increases from 0 to 90° . Due to an increased R_o , the energy efficiency drops significantly. Moreover, the 2nd efficiency peak is pushed into the lower PBO level and the PBO range for efficiency enhancement also reduces, further limiting the achievable average efficiency in modulation (e.g. high-order QAM and OFDM). From Figure 5-5b, a higher R_o results in a rapidly reduced dynamic range, indicating a larger φ ($>90^\circ$) is necessary to achieve a deeper PBO range, which is also predicted by earlier discussion on (5-17).

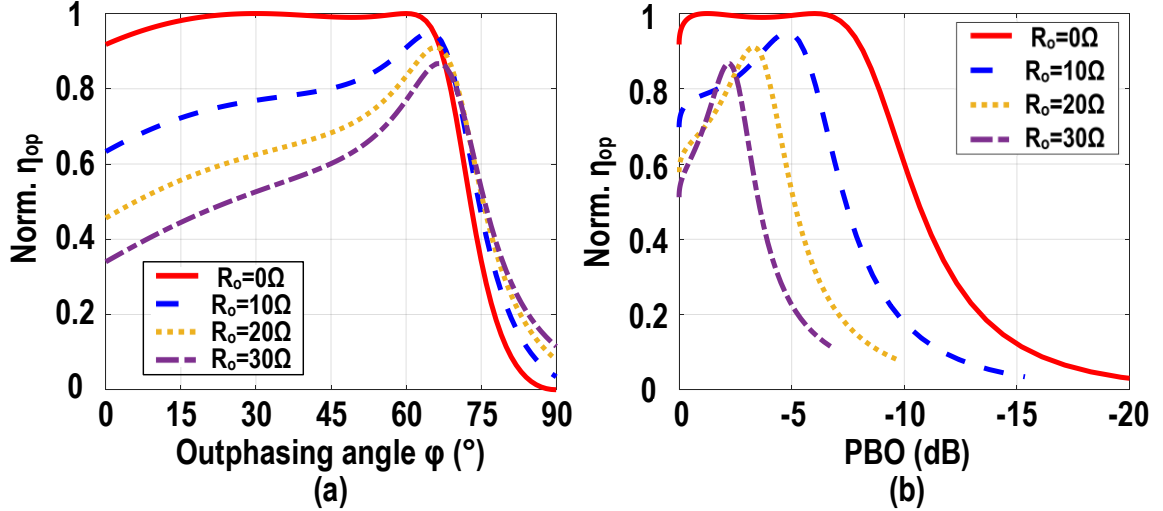


Figure 5-5 Theoretical outphasing efficiency η_{op} versus (a) φ and (b) PBO.

Following the theoretical analysis, the same PA cores (a CS and a cascode PA) from Figure 5-3b are used to further simulate the voltage-mode outphasing performance at 28GHz by including actual large-signal device models with layout parasitics. Ideal passives

are used in these simulations with the PAs driven by matched signal ports. The simulation results are summarized in Figure 5-6. As indicated by (5-17), a larger outphasing offset angle happens in the outphasing implementation with cascode PAs (Figure 5-5a), due to a larger output resistance. In addition, the deviation from the ideal φ -to-AM relationship necessitates additional signal predistortion to correct AM errors. The simulated PAE and AM-PM are shown in Figure 5-6b. With cascode PAs, the voltage-mode outphasing efficiency drops quickly, showing largely compromised PAE enhancement at PBO. Moreover, large AM-PM error is observed in outphasing with cascode PAs, which significantly complicates the digital predistortion (DPD) process and further limits the achievable modulation performance. Although an outphasing architecture with CS PAs exhibits a much better PAE versus PBO profile, it is worth noting that the PA-stage gain is deeply compressed at PBO (e.g. 8.5dB gain at 6dB PBO) due to the constant input driving strength (Figure 5-3b). If we consider the passive loss from the PA input matching in practice, the further reduced PA gain will lower the PBO efficiency even more. Additionally, the conventional voltage-mode outphasing architecture with CS PAs still shows a considerable amount of AM-PM distortion (e.g. 15° at 9dB PBO) that needs to be corrected through DPD.

In summary, conventional voltage-mode outphasing architecture primarily utilizes saturated linear PAs for practical implementations at mm-wave, while cascode (or further stacked) PA topology shows very limited PBO efficiency enhancement in an outphasing architecture due to their large output impedance, let alone their substantial nonlinearities introduced in outphasing operation. However, though saturated CS PAs can be used, the limited achievable output power, lower gain in compression and the resulting inferior PAE at PBO, and the large nonlinearities during saturation make mm-wave outphasing systems yet a big challenge in practice.

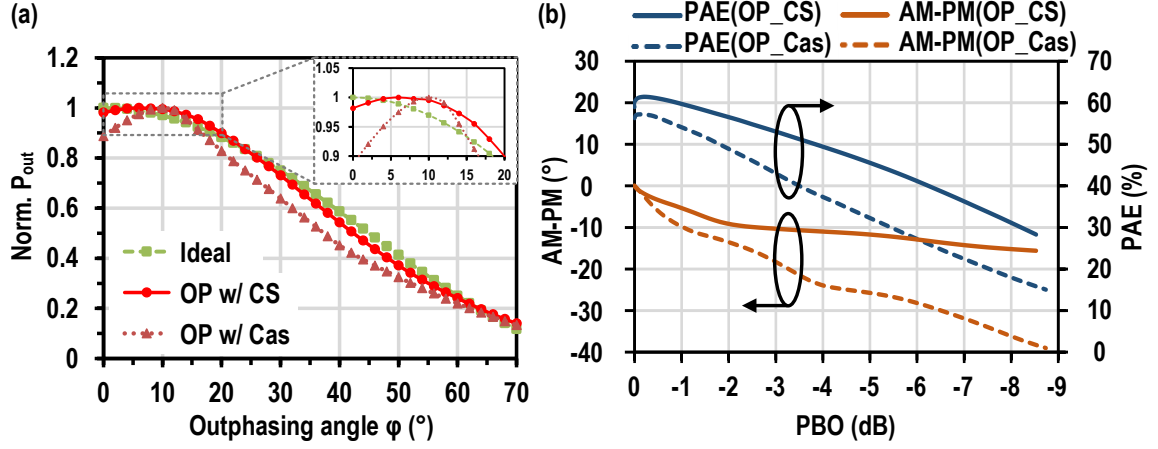


Figure 5-6 (a) Simulated P_{out} - ϕ dependence in an ideal case, and in outphasing with saturated linear (CS and cascode) PAs (OP w/ CS, and OP w/ Cas). (b) Simulated PAE and AM-PM versus PBO in both outphasing implementations with CS and cascode PAs.

5.3 Proposed Current-Mode Inverse Outphasing Architecture Employing a Parallel Power Combiner

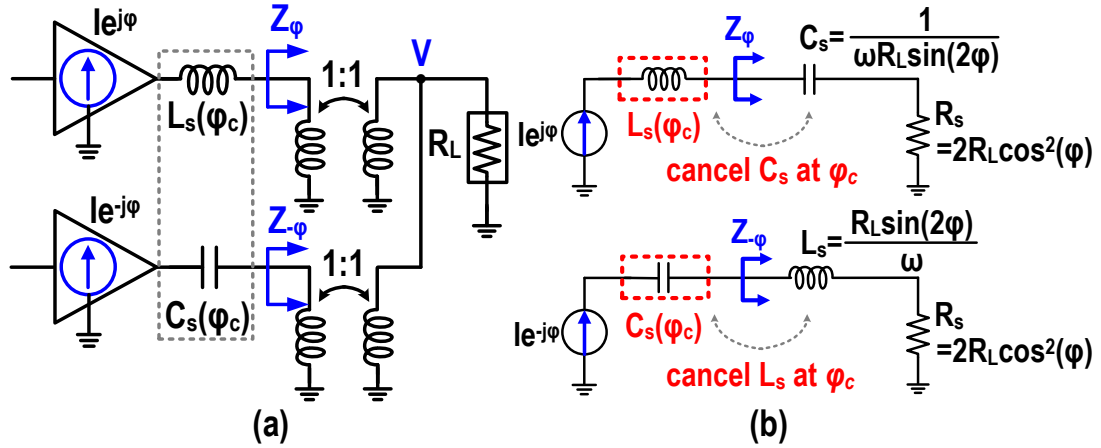


Figure 5-7 (a) Proposed current-mode inverse outphasing architecture. (b) Effective load impedances seen by each PA path.

From the analysis in Section 5.2, we realize that the lack of voltage-mode driving sources and their high output impedance at mm-wave are the major bottleneck for the conventional outphasing architecture. To address this challenge, an outphasing topology

that is based on current-mode linear analog PAs is highly desired. Therefore, we propose a current-mode inverse outphasing architecture that is a circuit duality of the conventional outphasing and is naturally compatible with mm-wave linear PAs with high output impedance [67]. Moreover, the series outphasing combiner is replaced by a much simpler and low-loss parallel power combining scheme that can be readily realized with current summing at mm-wave.

Figure 5-7a depicts the current-mode inverse outphasing structure that is driven by two outphased current sources ($Ie^{j\varphi}$ and $Ie^{-j\varphi}$). The parallel output network vectorially combines the two currents and generate an output voltage across R_L with a value of

$$V = (Ie^{j\varphi} + Ie^{-j\varphi})R_L = 2IR_L\cos(\varphi). \quad (5-21)$$

The output power can thus be expressed as

$$P_L = \frac{V^2}{2R_L} = 2I^2R_L\cos^2(\varphi). \quad (5-22)$$

To obtain the load impedances at each PA output, the Z-parameters (before adding the Chireix compensation) looking into the output network are derived as

$$Z_{\pm\varphi} = \frac{V}{Ie^{\pm\varphi}} = 2R_L[\cos^2(\varphi) \mp j\frac{1}{2}\sin(2\varphi)]. \quad (5-23)$$

Its real part captures a series load resistance (R_s) being actively modulated by the outphasing angle φ following

$$R_s = 2R_L\cos^2(\varphi). \quad (5-24)$$

Compared with the conventional voltage-mode outphasing active load modulation described by (5-6), R_s is controlled by φ in an inverse relationship ($1/\cos^2\varphi$ vs. $\cos^2\varphi$). Hence, we name this new architecture as inverse outphasing architecture. Similarly, there still exists a pair of reactive components associated with outphasing operation at each PA output. However, different from the shunt L_p and C_p compensation in the conventional outphasing structure, they appear in series with the load resistance R_s in this proposed outphasing architecture, as

$$C_s = \frac{1}{\omega \times \text{Im}(Z_\varphi)} = \frac{1}{\omega \times R_L \sin(2\varphi)}, \quad (5-25)$$

$$L_s = \frac{\text{Im}(Z_{-\varphi})}{\omega} = \frac{R_L \sin(2\varphi)}{\omega}. \quad (5-26)$$

As a result, series (instead of parallel) Chireix compensations are employed to cancel the reactance at a predetermined Chireix compensation angle φ_c . The effective load impedances seen by each PA are shown in Figure 5-7b. Following the above analysis, we notice many similarities between the conventional voltage-mode outphasing and our proposed current-mode inverse outphasing architectures. A detailed comparison is summarized in Table 5-1, from which it is clear that the inverse outphasing and the conventional outphasing architectures are circuit dualities.

Table 5-1 Comparison Between Outphasing and Inverse Outphasing

Properties	Outphasing	Inverse Outphasing
Driving sources	Voltage-mode sources	Current-mode sources
Output network	Series power combiner	Parallel power combiner
Analyzed parameters	Y-parameters	Z-parameters
Chireix compensations	Parallel L/C	Series L/C
Active load modulation	$\frac{1}{\cos^2(\varphi)}$	$\cos^2(\varphi)$

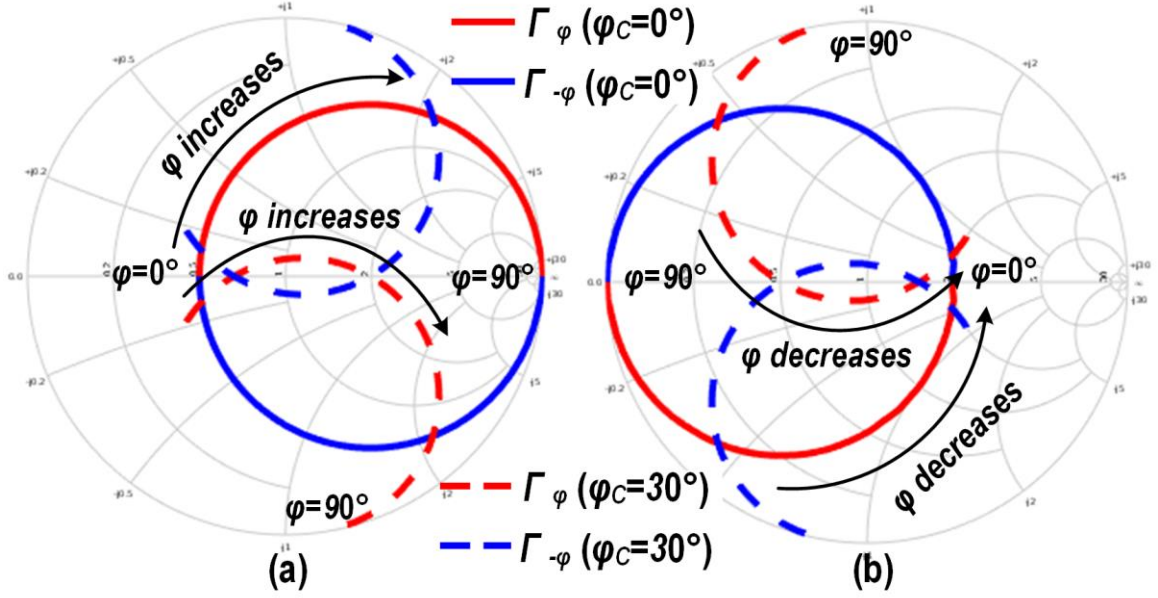


Figure 5-8 (a) Outphasing and (b) inverse outphasing active load modulation trajectory on Smith Chart (Γ_ϕ and $\Gamma_{-\phi}$ are the PA output reflection coefficients at the phase-leading and phase-lagging path).

The active load modulation trajectories on Smith Chart for both outphasing and inverse outphasing are shown in Figure 5-8. The scenarios with and without Chireix compensation ($\phi_C = 0^\circ$ and 30°) are also compared in the plot, validating its function. Interestingly, the load trajectories in the two cases (outphasing vs. inverse outphasing) are centrosymmetric with respect to the center of the Smith chart ($Z_o = R_L = 50\Omega$), which further demonstrates the duality behaviors. Since the PA loads are modulated in an opposite fashion, the outphasing angle ϕ of the proposed architecture should decrease for an increased load resistance at PBO, resulting in an inverse outphasing operation. At peak P_{out} , the inverse outphasing therefore operates at an initial outphased condition ($\pm\phi_i$), which in turn lowers down the PA load resistance by a factor of $\cos^2(\phi_i)$ based on (5-24) and particularly benefits high-power PA designs at mm-wave.

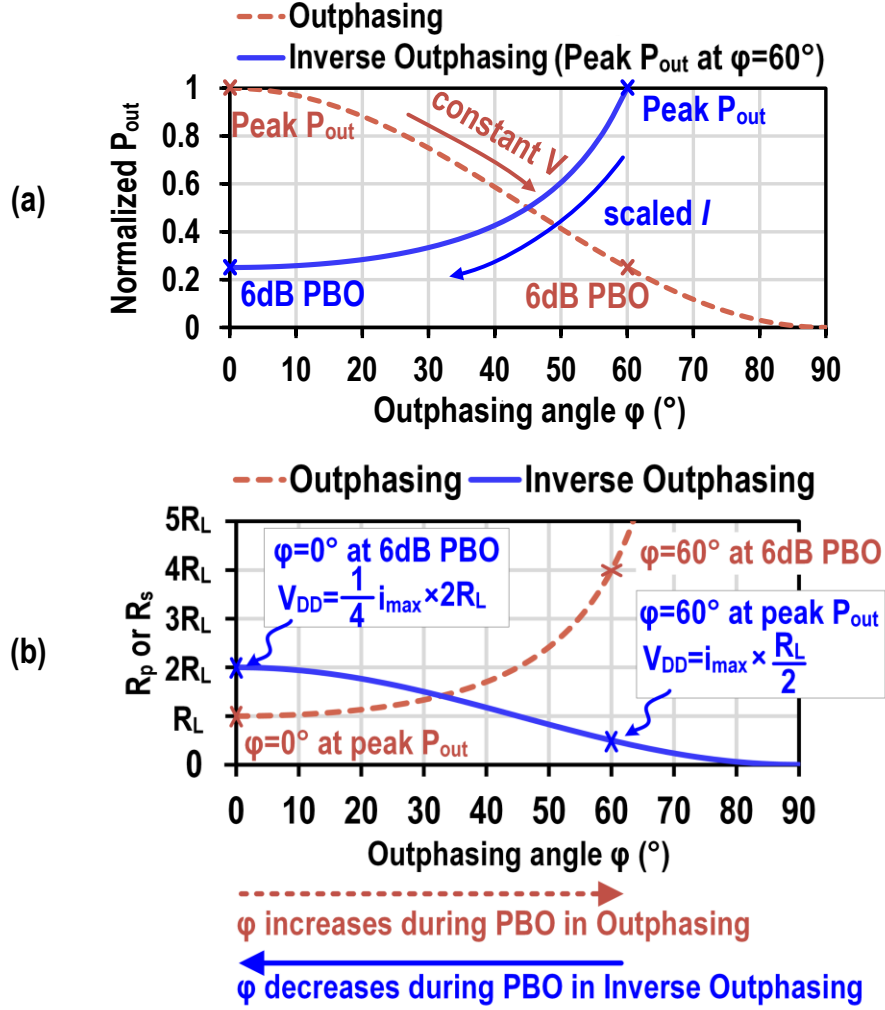


Figure 5-9 (a) P_{out} versus ϕ and (b) effective PA load resistance (R_p or R_s) in outphasing and inverse outphasing operation.

The operation principle is further illustrated in Figure 5-9. Compared to conventional outphasing with a constant PA output voltage swing and increasing ϕ for PBO (Figure 5-9a), the inverse outphasing employs decreasing ϕ and properly scaled driving current amplitude to realize PBO, and more importantly, to satisfy the load-line condition at PBO. Considering practical outphasing angles are often restricted within 60° ($\phi \leq 60^\circ$) to improve the efficiency and dynamic range, the PA load resistance R_p increases from R_L to $4R_L$ in the conventional voltage-mode outphasing (Figure 5-9b). In comparison, if we choose $\phi_i = 60^\circ$ for peak P_{out} in inverse outphasing, the PA should achieve its maximum

output voltage swing for optimal power/efficiency ($V_{DD} = i_{max} \times \frac{R_L}{2}$). At 6dB PBO where φ decreases to 0° , the driving current amplitude reduces by 4 \times , again realizing full PA output voltage swing ($V_{DD} = \frac{i_{max}}{4} \times 2R_L$) for the 2nd efficiency peak. Beyond 6dB PBO, the two PA branches operate as two in-phase analog PAs to achieve a large dynamic range as generic analog PAs.

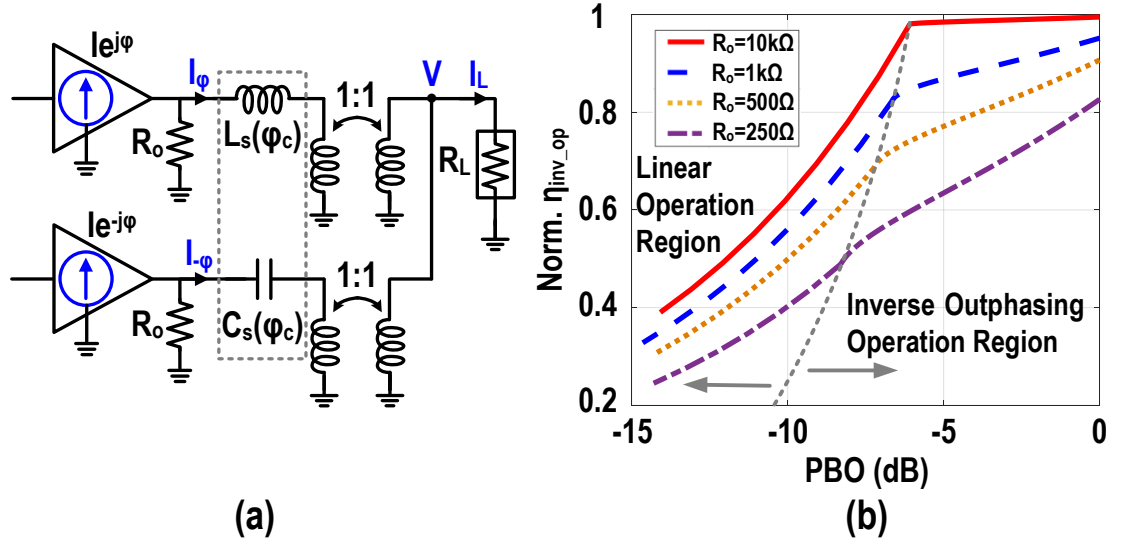


Figure 5-10 (a) Inverse outphasing architecture with finite PA output resistances. (b) Theoretical inverse outphasing efficiency versus PBO.

If the PA has finite output impedance R_o (Figure 5-10a), the PA output currents $I_{\pm\varphi}$ can be derived from

$$Ie^{j\varphi} - I_\varphi = \frac{I_\varphi Z'_L + I_L R_L}{R_o}, \text{ and} \quad (5-27)$$

$$Ie^{-j\varphi} - I_{-\varphi} = \frac{I_{-\varphi} Z'_C + I_L R_L}{R_o}, \quad (5-28)$$

where Z'_L and Z'_C are the impedances of the required series Chireix compensations in the inverse outphasing architecture. The output parallel power combiner realizes current summing, leading to

$$I_\varphi + I_{-\varphi} = I_L. \quad (5-29)$$

The complex conjugate relationship between Chireix compensations still holds, with

$$Z'_L + Z'_C = 0. \quad (5-30)$$

From (5-27)-(5-30), the load current I_L is thus solved as

$$I_L = \frac{2I[\cos(\varphi) + \frac{R_L}{R_o} \sin(2\varphi_c) \sin(\varphi)]}{1 + \frac{2R_L}{R_o} + \frac{R_L^2}{R_o^2} \sin^2(2\varphi_c)}. \quad (5-31)$$

Considering a driving current profile as

$$I = \frac{1}{4} \frac{i_{max}}{\cos^2(\varphi)} = \frac{V_{DD}}{2R_L \cos^2(\varphi)}, \quad (5-32)$$

where i_{max} is maximum PA output current amplitude. The inverse outphasing efficiency can therefore be calculated as

$$\eta_{inv_op} = \frac{P_L}{P_{DC}} = \frac{\frac{1}{2} I_L^2 R_L}{2V_{DD} I_{DC}} = \frac{\pi I_L^2 R_L}{8V_{DD} I}. \quad (5-33)$$

The theoretical inverse outphasing efficiency is plotted in Figure 5-10b. First, the dependence of the achievable efficiency on R_o shows that the high output impedance of

mm-wave high-power PAs (e.g. stacked PAs) is inherently accommodated by the proposed architecture. Within the inverse outphasing operation region, significant efficiency enhancement is achieved even with finite PA output impedance. When φ reduces to 0° , (in-phase) linear operation is employed, not only maintaining a large dynamic range, but also realizing a less steep efficiency roll-off at deeper PBO as compared to that in the conventional outphasing operation (Figure 5-5b).

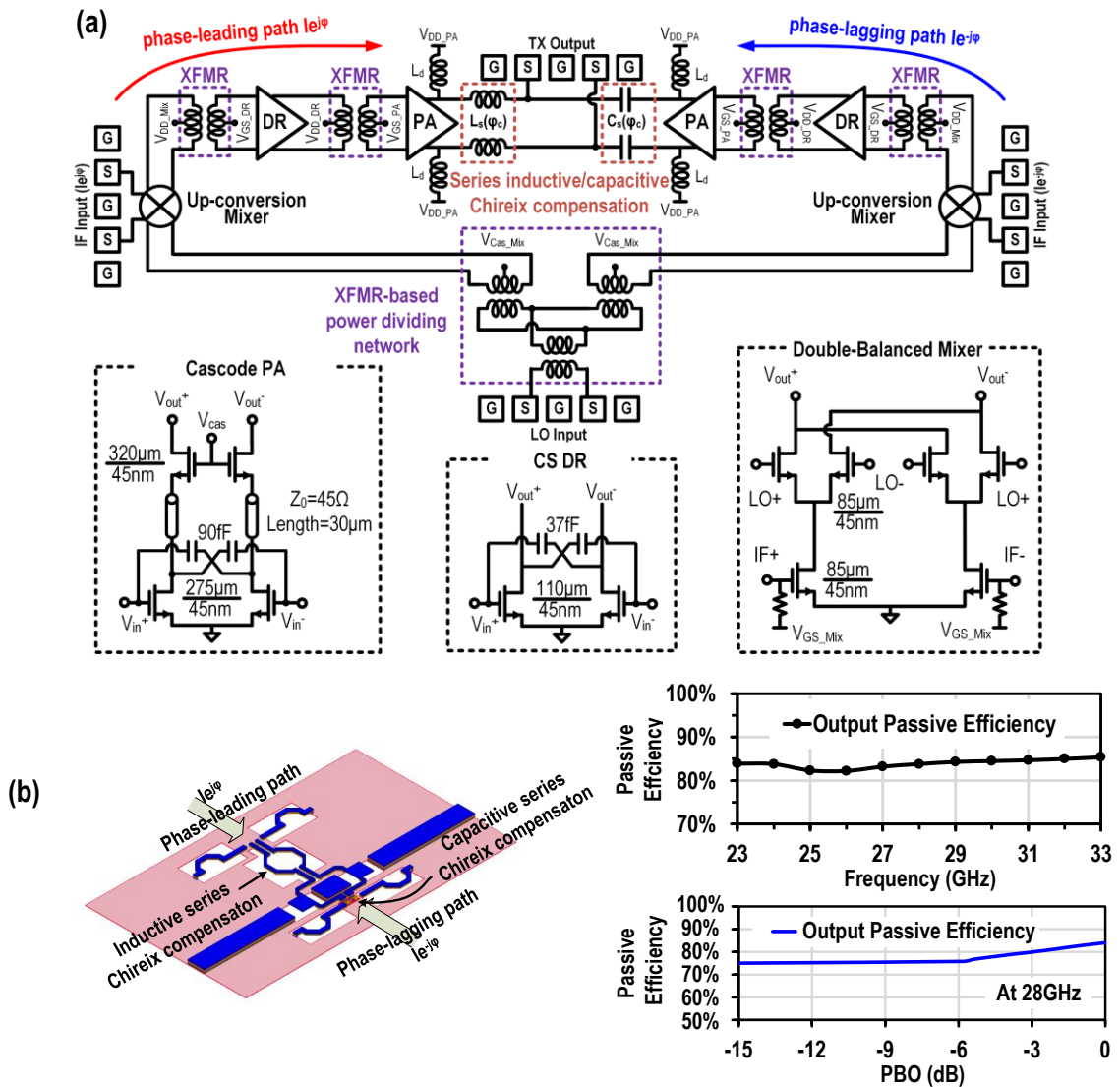


Figure 5-11 (a) Top-level circuit and building block schematic. (b) EM model of the output network and its simulated passive efficiency.

To demonstrate the proposed inverse outphasing architecture, we implement a 28GHz TX front-end as a proof-of-concept. The top-level circuit schematic is shown in Figure 5-11a. The phase-leading ($Ie^{j\varphi}$) and phase-lagging ($Ie^{-j\varphi}$) paths are parallelly combined with the series inductive and capacitive Chireix compensations implemented at the corresponding PA outputs. Each outphasing branch consists of a cascode PA, a CS driver (DR), and an up-conversion mixer. Transformers are employed as inter-stage matching networks with their center-taps properly terminated for biasing and common-mode stability. In addition, a transformer-based power dividing network is designed for LO distribution.

A cascode PA is used for its higher P_{out} and power gain. More importantly, its high output impedance is naturally compatible with the inverse outphasing architecture. A CS DR is implemented with its size, biasing, and supply optimized for a better overall efficiency while still providing sufficient driving strength. Capacitive neutralization is employed on both PA and DR for improved differential power gain and stability. The double-balanced mixers up-convert the 5GHz IF outphasing signals to the 28GHz carrier. The on-chip implementation of mixers minimizes the phase/amplitude mismatch between the two outphasing paths. The EM model of the output network and its simulated passive efficiency are shown in Figure 5-11b. The output network including the Chireix compensations achieves over 80% passive efficiency (i.e. <1dB signal loss) at P_{sat} across frequency, and moreover, maintains above 75% passive efficiency across the entire PBO range.

5.4 Measurement Results

5.4.1 Continuous-Wave Measurement

The TX chip is fabricated in the GlobalFoundries 45nm CMOS SOI process, with a core area of 0.6mm by 1.6mm (Figure 5-12a). The continuous-wave (CW) measurement setup is depicted in Figure 5-12b. Two channels of a 4-channel Keysight 8195 arbitrary waveform generator (AWG) are used to generate the input IF outphasing signals, with an external signal source providing the LO for the TX chip (Figure 5-12b). To measure the output power, a power meter and sensor are used to capture the up-converted carrier power. For the nonlinearity testing, the TX output is first attenuated, down-converted by the same LO, amplified, and then sent to a real-time sampling oscilloscope where it is compared with a coherent reference matching signal for AM-AM and AM-PM measurement. The reference signal and the trigger signal for the sampling oscilloscope are provided by the other two AWG channels.

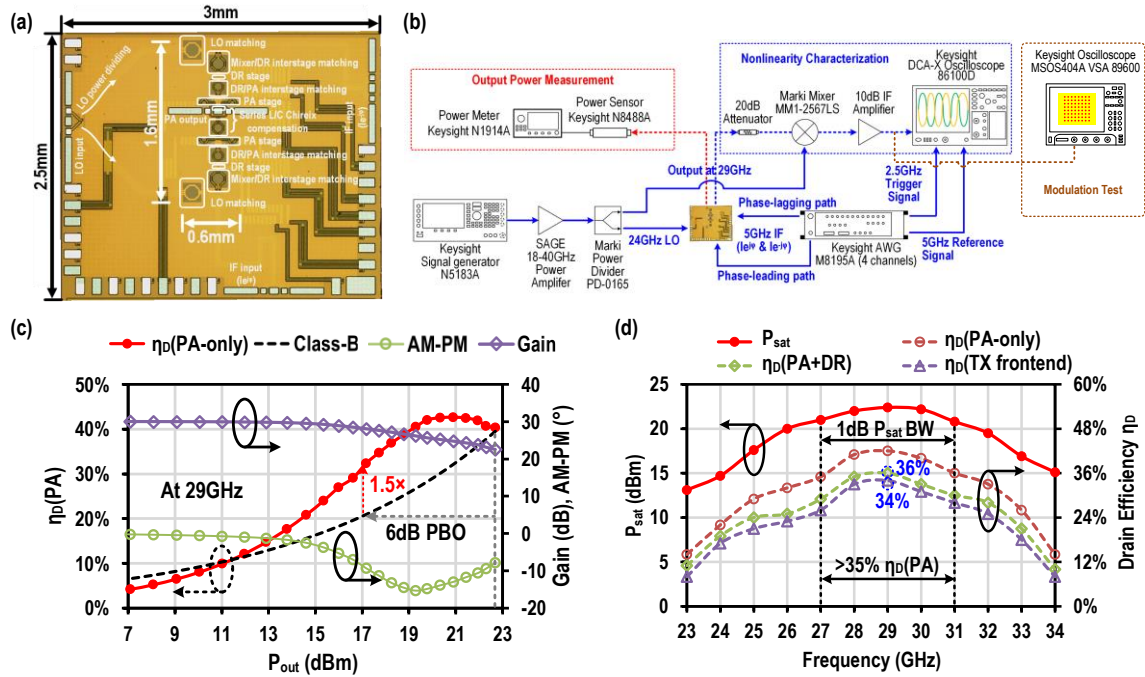


Figure 5-12 (a) Chip microphotograph of the inverse outphasing TX. (b) The CW and modulation measurement setup for output power and nonlinearity characterizations. (c) The TX large-signal performance at 29GHz. (d) The frequency response of the inverse outphasing TX.

The measured TX large-signal performance at 29GHz is shown in Figure 5-12c. A P_{sat} value of 22.7dBm is measured with 42.6% peak PA drain efficiency (η_D) and 31% PA η_D at 6dB PBO. It demonstrates 1.5 times efficiency enhancement over an ideal Class-B PA, verifying the proposed inverse outphasing active load modulations. The AM-AM and AM-PM are also characterized, based on which a memoryless 2-dimentional (P_{in} , φ) lookup table (LUT) is created and later used to provide the desired input outphasing signals and correct the nonlinearity distortion in the modulation testing. The frequency response of the inverse outphasing TX is plotted in Figure 5-12d. It achieves 1dB P_{sat} bandwidth from 27 to 31GHz, where the PA maintains over 35% η_D . The TX delivers more than 20dBm P_{out} from 26 to 32GHz, and keeps above 32% PA-only, 25% PA plus DR, and 23% total TX front-end η_D , respectively.

5.4.2 Modulation Test

To ensure high-fidelity modulations, the TX large-signal nonlinearities (AM-AM and AM-PM) are first calibrated and then corrected through LUT-based static DPD. Compared with existing outphasing PAs/TXs, no additional computation resources are required to perform inverse outphasing operation. Essentially, the same CW measurement setup should be used to preserve the validity of the nonlinearity characterization, with only the sampling oscilloscope replaced with a mixed-signal oscilloscope for digital demodulation (Figure 5-12b).

The 64-QAM demodulated constellations and spectra at different modulation bandwidth are shown in Figure 5-13a. When transmitting 3Gb/s 64-QAM signals, the inverse outphasing TX achieves 16dBm average P_{out} (P_{avg}) and 23.8% PA average η_D ($\eta_{D_{avg}}$), with -25.3dB EVM and around -29.5dBc ACLR. The EVM is referenced to the RMS amplitude of the constellation. Up to 15Gb/s data rate is demonstrated for 64-QAM signals. At the maximum modulation speed, the TX still maintains 15.6dBm P_{avg} and

22.5% PA η_{D_avg} , with -22.5dB EVM and -29.2dB ACLR. The TX performance under modulation testing (P_{avg} , PA η_{D_avg} , EVM and ACLR) with 64-QAM signals is further summarized in Figure 5-13b and 13c. Over the modulation bandwidth, the TX consistently delivers over 15dBm P_{avg} and keeps above 22% PA η_{D_avg} , while preserving a sufficient signal fidelity (EVM and ACLR). Additional modulation schemes such as 16- and 256-QAM are also tested with the TX, shown in Figure 5-13d. Consistent modulation performance is achieved under different modulation schemes, demonstrating state-of-the-art PA/TX performance in dynamic operations, and further validating the inverse outphasing approach.

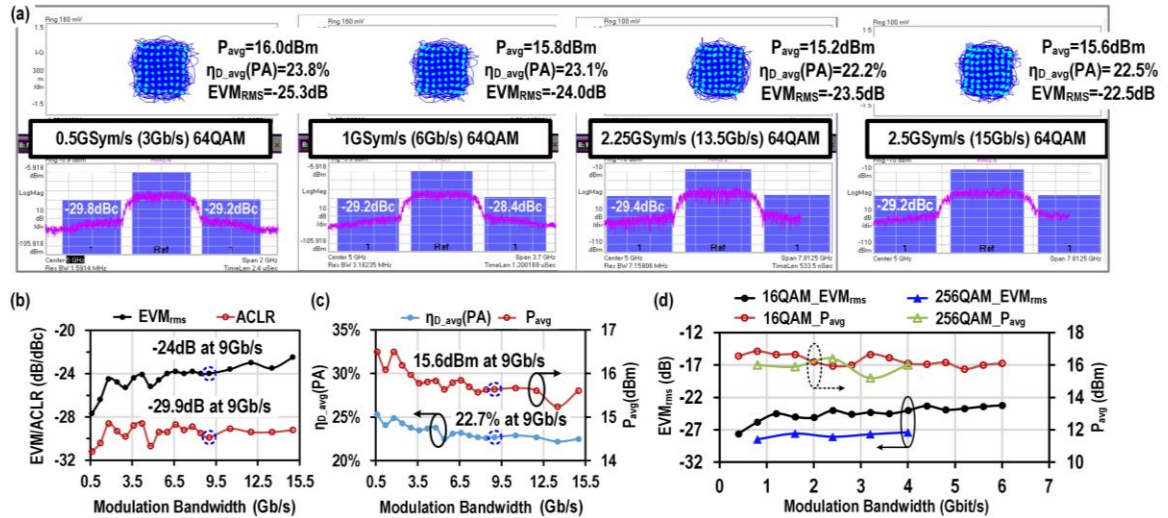


Figure 5-13 (a) Demodulated 64QAM constellations and spectra at different modulation bandwidth. (b) EVM and ACLR of 64QAM versus modulation bandwidth. (c) Average output power and PA drain efficiency versus modulation bandwidth. (d) 16- and 256-QAM modulation testing results.

Table 5-2 compares this work with the state-of-the-art silicon-based TX/PA performance at similar frequencies. It not only achieves a high output power and peak efficiency, but also realizes significant efficiency enhancement at PBO. Moreover, up to 15Gb/s data rate with high-order QAM is demonstrated in modulation test, delivering one

of the highest reported average output power and maintaining a competitive average efficiency.

Table 5-2 Comparison with State-of-The-Art Mm-Wave Silicon-Based PAs/TXs

	mm-Wave Outphasing TX/PA				mm-Wave Doherty PA			mm-Wave Analog/Digital PA		
	This work	Ning JSSC'20	Rabet ISSCC'18	Li JSSC'19	Indrayanti RFIC'17	Hu ISSCC'17	Wang ISSCC'19	Shakib ISSCC'17	Li ISSCC'18	Chappidi JSSC'18
Technology	45nm CMOS SOI	45nm CMOS SOI	130nm SiGe	45nm CMOS SOI	28nm CMOS	130nm SiGe	45nm CMOS SOI	40nm CMOS	130nm SiGe	130nm SiGe
Architecture	Inverse Outphasing TX	Outphasing PA with current-mode combiner	Triaxial Balun Outphasing PA	On-Antenna Outphasing TX	Analog Doherty PA	Multiband Analog Doherty PA	Mixed-Signal Doherty PA	Analog PA	Harmonically Tuned PA	Digital Asymmetrical PA
TX or PA	TX	1-Stage PA	1-Stage PA	TX	2-Stage PA	2-Stage PA	2-Stage PA	2-Stage PA	2-Stage PA	2-Stage PA
Supply (V)	2.0 (PA and Mixer), 1.0 (DR)	1.2	4	1.0 (PA and DR), 2.0 (Mixer)	1.0	1.5	2.0	1.1	1.9	4.0
Frequency (GHz)	29	30	28	28	32	28	27	27	28.5	40
Gain (dB)	30 (TX)	7	14.0	N.A.	22	18.2	19.1	22.4	20	23.4
P_{sat} (dBm)	22.7	17	23	17.1	19.8	16.8	23.3	15.1	17	23.7
Peak PAE	42.6% η_D (PA), *41.3% PAE(PA)	**50.5% η_D (PA)	**41.4%	43%	21%	20.3%	40.1%	33.7%	43.5%	28.5%
PAE@PBO	31% η_D (PA), *30.6% PAE(PA) @6dB PBO	**40% η_D (PA) @6dB PBO	**34.7% @6dB PBO	23% @6dB PBO	4% @6dB PBO	13.9% @5.9dB PBO	33.1% @6dB PBO	15.1% @5dB PBO	20% @6dB PBO	14.8% @6dB PBO
Modulation scheme	64-QAM	64QAM	64-QAM OFDM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM OFDM	64-QAM	16-QAM
Data rate (Gb/s)	3/6/12/15	0.6/3	0.48	6	15	6	15	4.8	18	4
EVM* (dB)	-25.3/-24/-23.6/-22.5(RMS)	-36.4/-28(RMS)	-30.5(RMS)	-26.2(RMS)	-25(Peak)	-26.6(Peak)	-24(RMS)	-25(RMS)	-25(Peak)	-18.2(Peak)
ACLR (dBc)	-29.8/-29.4/-29.4/-29.2	-28/-26.4	-33	-28.3	-20	-25.4	N.A.	-29.4	N.A.	-25
P_{avg} (dBm)	16/15.8/15.6/15.6	N.A./10.2	14.3	10.7	11.7	7.2	15.0	6.7	9.8	16.4
PAE _{avg}	23.8%/23.1%/22.7%/22.5% η_D (PA)	N.A./**31.2% η_D (PA)	**25.3%	20.6%	5.75%	14.4% η_C	26.4%	11%	18.4	19.9% η_C
Area (mm ²)	±0.96	1.65	0.56	115	±0.59	1.76	±0.52	±0.225	±0.29	±0.96

*When referenced to the RMS value of the constellation magnitudes, $EVM_{RMS} = EVM_{peak} + 3.7$ dB for 64QAM, where EVM_{peak} is referenced to the peak magnitude of the constellation.

**Single stage PA. †With on-package antenna. ‡Core area. η_{CD} =Collector/Drain efficiency

†PAE calculated based on simulated PA-stage power gain.

5.5 Conclusion

This chapter presents an in-depth study on the conventional voltage-mode outphasing and the proposed current-mode inverse outphasing architectures with closed-form design equations on their performance, including active load modulation, Chireix compensations, and achievable efficiency. This study elucidates the fundamental limits in the conventional outphasing and the advantages of the inverse outphasing especially at mm-wave. The theoretical analysis also reveals a duality relationship of the two outphasing schemes, offering new design insights. As a proof-of-concept, a 28GHz inverse outphasing TX is implemented in a 45nm CMOS SOI process, achieving high-efficiency outphasing operations with current-mode PAs. The TX measures 22.7dBm P_{sat} with 42.6% peak η_D and a significant 1.5× efficiency boost at 6dB PBO versus an ideal Class-B PA. The TX

supports >10Gb/s high-order QAM signals with the state-of-the-art modulation performance.

CHAPTER 6. MULTI-FEED ANTENNA AND ELECTRONICS

CO-DESIGN: AN E-BAND ANTENNA-LNA FRONT-END WITH ON-ANTENNA NOISE-CANCELING AND GM-BOOSTING

6.1 Introduction

Merging antennas with front-end electronic circuits recently have created a new design paradigm to facilitate front-end innovations and advance circuit performance beyond existing electronics-only designs [68]-[83]. Different from conventional approaches that view antennas simply as a single-feed 50Ω radiation load, we exploit antennas as multi-feed passive radiating networks that concurrently interface with multiple front-end circuits, breaking the imposed single-feed boundary between antennas and electronics (Figure 6-1). By judiciously controlling the driving signals or termination conditions of the multiple electronics, desired near-field current/voltage (I/V) can be actively synthesized to realize target far-field characteristics [13]. Note that this is also different from the concept of “Active Antennas”, since the active circuits are not used to compensate the signal loss caused by the antenna-size-to-wavelength mismatch [72]-[76]. Moreover, antenna-electronics co-designs can be explored for a wide variety of on-antenna signal processing and conditioning functionalities. On-antenna power combining eliminates the lossy power combining network at the output of power amplifiers (PAs) or transmitters (TXs), boosting the total output power (P_{out}), equivalent isotropic radiated power (EIRP), and system efficiency. Unlike spatial power combining using antenna arrays, on-antenna power combining maintains a single-antenna footprint without large antenna panels. It also obviates beamwidth reduction and eases TX-RX alignments in mobile dynamic applications. In addition, TXs with on-antenna power combining can be

placed in an array for further spatial combining and beam-forming. Going beyond on-antenna power combining, multi-feed antennas for on-antenna Doherty and outphasing active load modulations are also explored, achieving the state-of-the art PA/TX energy efficiency at power back-off (PBO). Furthermore, inherently wideband feed isolation can be exploited in multi-feed antennas to realize mm-Wave polarization-division-duplex wireless links supporting Gbit/s complex modulated signals with chip-to-chip demonstrations [83], [84]. Multi-feed antennas as well as electronics co-designs have also been explored for signal generation and receiver of THz “invisible sensor” nodes [39].

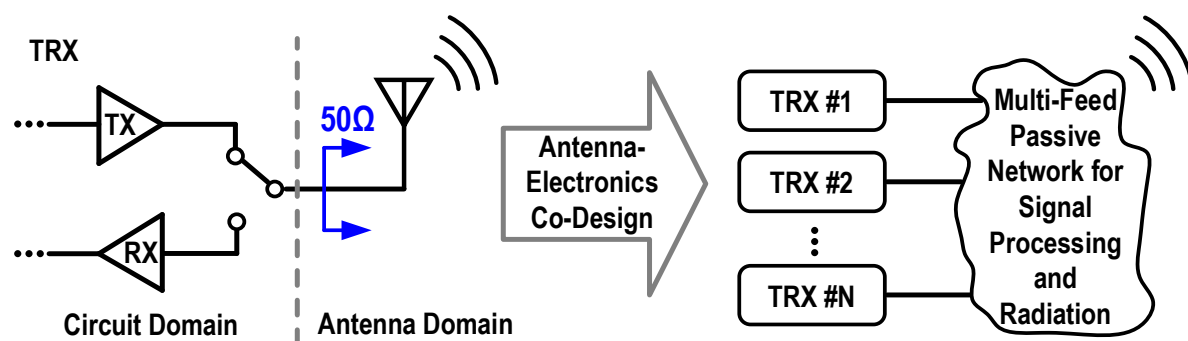


Figure 6-1 Conventional separate circuit and antenna design domain with 50Ω standard interface, and a co-design strategy enabling interactions among multiple TRXs on antenna.

The antenna-electronics co-design and multi-feed antennas are particularly suitable for mm-Wave frontends, due to compact on-chip/-package antennas and co-located electronic circuits, and the resultant performance improvements are essential for many wireless applications like 5G and 5G-beyond communication and sensing.

Presently, much research effort on antenna-electronics co-design has been focused on TXs, while there are limited explorations on the receiver (RX) architectures. This paper explores the feasibility of extending the antenna-electronics co-design concept to RX topology innovations, aiming at improving key RX performance, such as noise figure (NF) and linearity. As a proof-of-concept, we propose an on-antenna LNA noise-canceling and

gm-boosting scheme [87]. It is prototyped in GlobalFoundries 45nm CMOS SOI process with high-resistivity substrate to support high-efficiency on-chip antenna implementations. The target frequency is E-band, where RXs with high sensitivity and linearity, and wide bandwidth are necessary, while integration with on-chip antennas can minimize interconnection loss and parasitics.

This chapter is organized as follows. Section 6.2 presents our theoretical analysis and proposed equivalent circuit models that capture the circuit behaviors of multi-feed antenna systems at their feed terminals, fundamentally as series, parallel, or hybrid circuit connections with different scaling. Section 6.3 presents the proposed on-antenna noise-canceling and gm-boosting antenna-LNA structures with the circuit equivalent modeling of the multi-feed antenna network. Section 6.4 demonstrates the implementation of the E-band antenna-LNA front-end. The experimental results are summarized in Section 6.5. Section 6.6 finally concludes this chapter.

6.2 Circuit Modeling of Multi-Feed Antenna Systems

A generic multi-feed antenna system is intrinsically a cross-domain system composed of multiple electronic frontends interfacing with one or multiple near-field coupled antennas. Although an antenna-electronics systems can be accurately captured using 3D full-wave EM simulators, such a purely EM approach however does not reveal adequate design insights and has limited use in guiding antenna-electronics co-designs and innovations. To that end, in this section, we propose and theoretically validate the equivalent circuit models of various multi-feed antenna systems, which will offer straightforward design intuitions and further our understanding of such antenna-electronics coupled systems.

It is recognized that the driving behaviors of the antenna network is equivalent to an N-port passive non-isolating circuit network with the radiation effect as an implicit load,

and therefore can be represented by a circuit model. Based on the types of the standing-wave antenna, the terminal signals can be viewed as being processed in either voltage (E -field) or current (J -field) domain on the antenna. As a result, the multi-feed antenna systems can be fundamentally categorized as series (support independent feed/terminal voltages), parallel (support independent feed/terminal currents), or hybrid configurations. Since the multi-feed antennas are built upon standing-wave antennas in our proof-of-concept demonstrations, the signals (V or I) at each antenna feed are in phase.

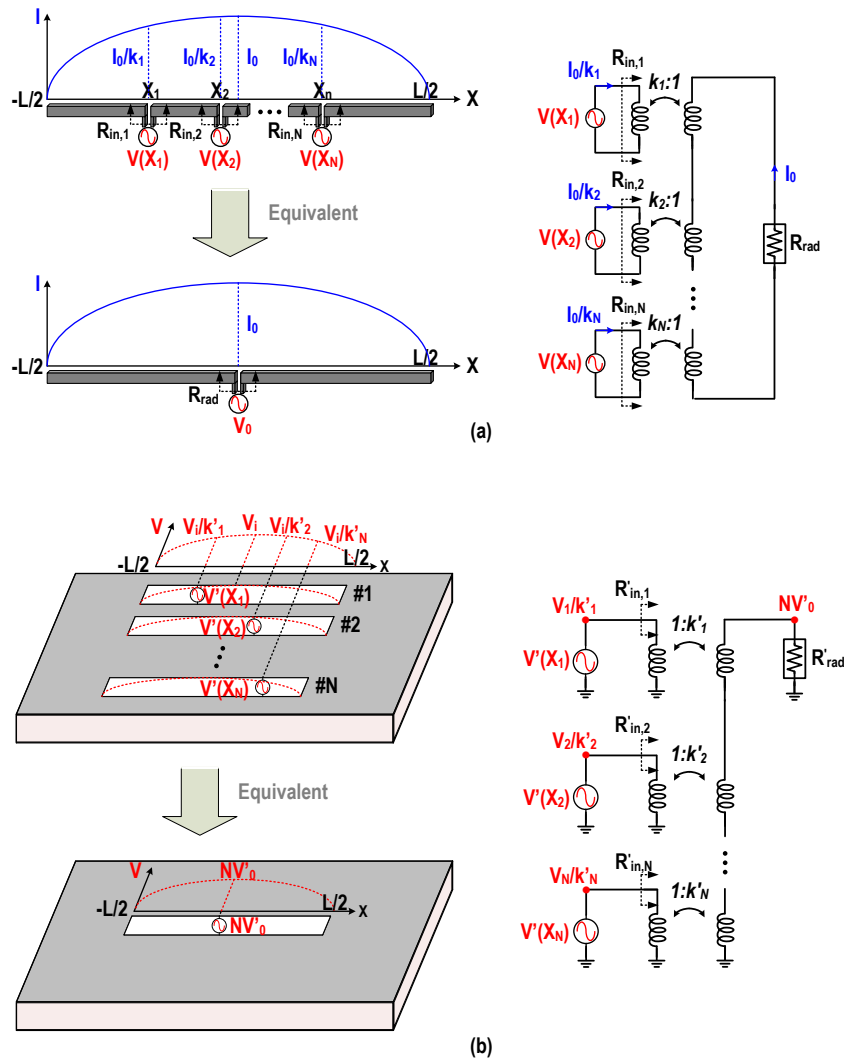


Figure 6-2 Series network configurations realized by (a) multi-feed current-mode antennas and its equivalent circuit model, and (b) multiple voltage-mode antennas and its equivalent circuit model.

6.2.1 Multi-Feed Antennas in A Series Network Configuration

The series network configuration of multi-feed antennas is defined as the cases that support independent voltages at different feeds or terminals. Typical examples of such configuration include implementing multiple feeds on various current-mode antenna (e.g. dipole and wire loop antennas) or near-field coupling multiple voltage-mode antennas (e.g. slot and aperture antennas) (Figure 6-2). The impedance behaviors at different feeds depend on the collective driving conditions (in transmitting) or termination conditions (in receiving) following the antenna duality principle [13]. Although there are infinite combinations of such collective multi-feed conditions, often one seeks to synthesize an identical on-antenna I/V distribution and thus the same far-field radiation in a multi-feed antenna system as that in a conventional single-feed antenna prototype. Assuming the total radiated power remains unchanged and antennas are lossless, in the current-mode antenna case (Figure 6-2a), the feed impedance relationship is expressed as

$$\frac{1}{2} I_0^2 R_{rad} = \sum_1^n \frac{1}{2} I^2(X_i) R_{in,i} \quad (6-1)$$

where I_0 is the current amplitude at the center of the dipole; R_{rad} is the driving impedance of the conventional single-feed antenna prototype; $I(X_i)$ and $R_{in,i}$ are the current amplitude and antenna input impedance at the i -th feeding location. It is well known that the current distribution on a 0.5λ dipole antenna (or voltage distribution on a 0.5λ slot dipole antenna) follows

$$I(x) \text{ or } V(x) = I_0(\text{or } V_0) \sin \left[k \left(\frac{L}{2} - |x| \right) \right] \text{ and } -\frac{L}{2} \leq x \leq \frac{L}{2} \quad (6-2)$$

where k is the wavenumber, $L = 0.5\lambda$ is the length of the (slot) dipole, and V_0 is the maximum voltage amplitude on the slot. As a result, $I(X_i)$ and the corresponding

transformation ratio k_i (Figure 6-2a) can be easily obtained from (6-2). When all the antenna feeds are implemented at the center of the dipole antenna, $I(X_i) = I_0$ and (6-1) is simplified into a more intuitive result, as

$$R_{in,i} = R_{rad}/N \quad (6-3)$$

where N is the total number of the feeds/paths. Equation (6-3) verifies the impedance behavior in a series power combining/splitting operation. Generally, the input impedance at any antenna feed is given by (Figure 6-2a)

$$R_{in,i} = \frac{V(X_i)}{I_0/k_i} = \frac{V(X_i) \times k_i}{\sum_1^N V(X_i) / R_{rad}} = \frac{V(X_i) \times k_i \times R_{rad}}{\sum_1^N V(X_i)} \quad (6-4)$$

showing the active load modulation behaviors among the antenna feeds, since the input impedance at a certain port is modulated by the driving strength to all other terminals. Such property has been leveraged to realize on-antenna Doherty [55], [56] and outphasing [60] active load modulation. In addition, since $I(X_i)$ (or equivalently k_i) varies at different feed locations, this dependence spatially modulates the driving impedance of each feeds and thus behaves as placing an implicit on-antenna transformer at each feed that passively scales the impedance and current/voltage. This property is leveraged in the reported multi-feed antenna-electronics co-designs [56], [87] and our proposed antenna-LNA co-design in Section 6.3.

Following the same principle, in the voltage-mode antenna case (Figure 6-2b) where N slot-dipoles are near-field coupled, we can obtain

$$\frac{1}{2} \frac{(NV'_0)^2}{R'_{rad}} = \sum_1^n \frac{1}{2} \frac{V'^2(X_i)}{R'_{in,i}} \quad (6-5)$$

When all the antenna feeds are implemented at the center of the slots with identical driving strength, we have

$$\frac{1}{2} \frac{(NV'_0)^2}{R'_{rad}} = N \frac{1}{2} \frac{V_0'^2}{R'_{in,i}}, \text{ when } V'(X_i) = V'_0 \quad (6-6)$$

which can be further simplified, and eventually arrive at the same conclusion as (6-3), demonstrating equivalent series connection among multiple feeds. Similarly, the general input impedance at any antenna feed in the implementation with voltage-mode antennas (Figure 6-2b) is expressed as

$$R'_{in,i} = \frac{V'(X_i) \times R'_{rad}}{\sum_1^N V'(X_i) \times k'_i} \quad (6-7)$$

In [26] and [37], series connection with power combining is realized utilizing a two-feed 1λ wire loop antenna (current-mode type) to achieve on-antenna series Doherty and outphasing for PA efficiency enhancement at PBO. Alternatively, [81] has demonstrated antenna-level series power combining with 16 near-field coupled slot elements (voltage-mode type), boosting the radiator EIRP at E-band in silicon.

6.2.2 Multi-Feed Antennas in A Parallel Network Configuration

Multi-feed antennas can also be configured as a parallel network that supports independent currents at different feeds or terminals. Such parallel network configurations are typically realized through implementation of multiple feeds on voltage-mode antennas (Figure 6-3a) or near-field coupled current-mode antennas (Figure 6-3b), showing an interesting duality behavior when compared with the series operations discussed in Section 6.2.1.

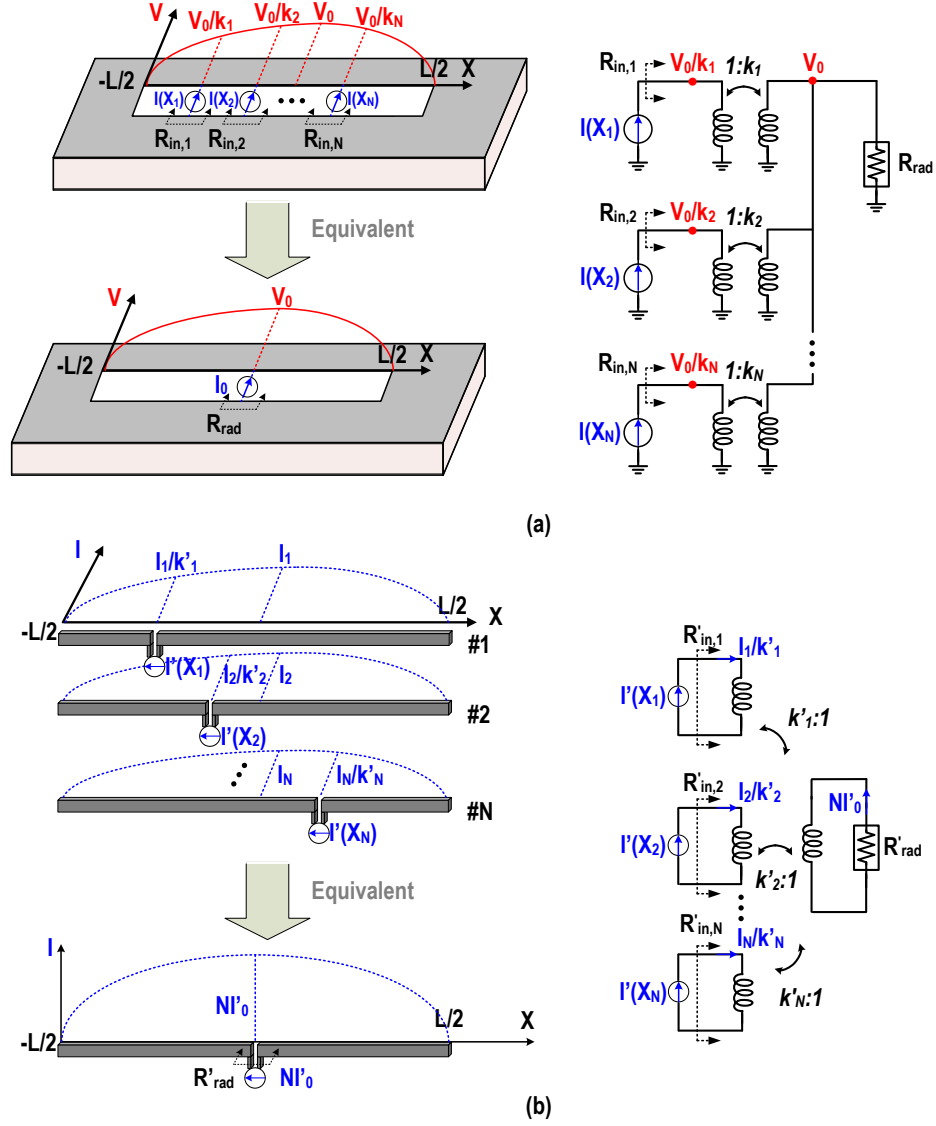


Figure 6-3 Parallel network configurations realized by (a) multi-feed voltage-mode antennas and its equivalent circuit model, and (b) multiple current-mode antennas and its equivalent circuit model.

Still assuming an unchanged on-antenna I/V distribution with multiple feeds employed on the lossless antennas, in the voltage-mode case (Figure 6-3a), the driving impedance follows

$$\frac{1}{2} \frac{V_0^2}{R_{rad}} = \sum_{i=1}^n \frac{1}{2} \frac{V^2(X_i)}{R_{in,i}}, \quad (6-8)$$

A more intuitive conclusion can be drawn when all the antenna feeds are implemented at the center of the slot antenna, leading to

$$R_{ini} = N \times R_{rad}, \quad \text{when } V(X_i) = V_0. \quad (6-9)$$

The input impedance at each port is effectively upscaled by a factor of N , validating the impedance behavior in a parallel power combining/splitting operation. In general, the input impedance at any antenna feed is given by (Figure 6-3a)

$$R_{in,i} = \frac{V_0/k_i}{I(X_i)} = \frac{\sum_1^N I(X_i) \times R_{rad}}{I(X_i) \times k_i} \quad (6-10)$$

further verifying the active load modulation behaviors among the antenna feeds in a parallel network configuration. For example, [4] demonstrates four-way parallel power combining using an on-chip slot antenna. Likewise, when N closely placed dipoles near-field coupled together, we find that

$$\frac{1}{2} (NI'_0)^2 R'_{rad} = \sum_1^n \frac{1}{2} I'^2(X_i) R'_{in,i}, \quad (6-11)$$

When all the antenna feeds are implemented at the center of the dipoles with identical driving strength, we have

$$\frac{1}{2} (NI'_0)^2 R'_{rad} = N \frac{1}{2} I'^2_0 R'_{in,i}, \quad \text{when } I'(X_i) = I'_0. \quad (6-12)$$

leading to the same conclusion as (6-9). As a result, it is an alternative example achieving antenna-level equivalent parallel connection among multiple feeds. Likewise, the general

input impedance at any antenna feed in the implementation with current-mode antennas (Figure 6-3b) is expressed as

$$R'_{in,i} = \frac{\sum_1^N I'(X_i) \times R'_{rad} \times k'_i}{I'(X_i)}. \quad (6-13)$$

In summary, the resonant antenna with a standing-wave I/V pattern is exploited as an I/V transformer, which can be further utilized to realize on-antenna series and parallel network configurations. By identifying its nature, the equivalent circuit modeling can thus be derived, which will be further discussed in the following sections.

6.2.3 EM Verification of the Proposed Circuit Modelling

To verify the validity of the proposed circuit modeling, 3-D full-wave EM simulations are performed using on-chip 0.5λ slot antennas as an antenna prototype. Without loss of generality, four feeds are implemented to achieve either a series connection configuration (Figure 6-4a) or a parallel connection configuration (Figure 6-4c). The 0.5λ slot antennas are designed at E-band using the BEOL of GlobalFoundries 45nm CMOS-SOI process with high resistivity substrate [88].

In Figure 6-4a, four feeds are employed on four near-field coupled slot antennas. All the four feeds are the center, and the slot antennas are identical for simplicity. From earlier discussion, its feed behavior follows a series connection network (Figure 6-2b). A conventional single-feed 0.5λ slot antenna is also simulated and its input impedance is plotted in Figure 6-4b, showing $R_{in_1feed} = 193\Omega$ at the center frequency. When the four feeds in Figure 6-4a are driven simultaneously with identical coherent signals, the input impedance at each feed (R_{in_4feed} at resonance in Figure 6-4b) becomes 47Ω , effectively reduced by approximately 4 times. Thus, the 3D EM simulations verify the equivalent series network connections among the feeds.

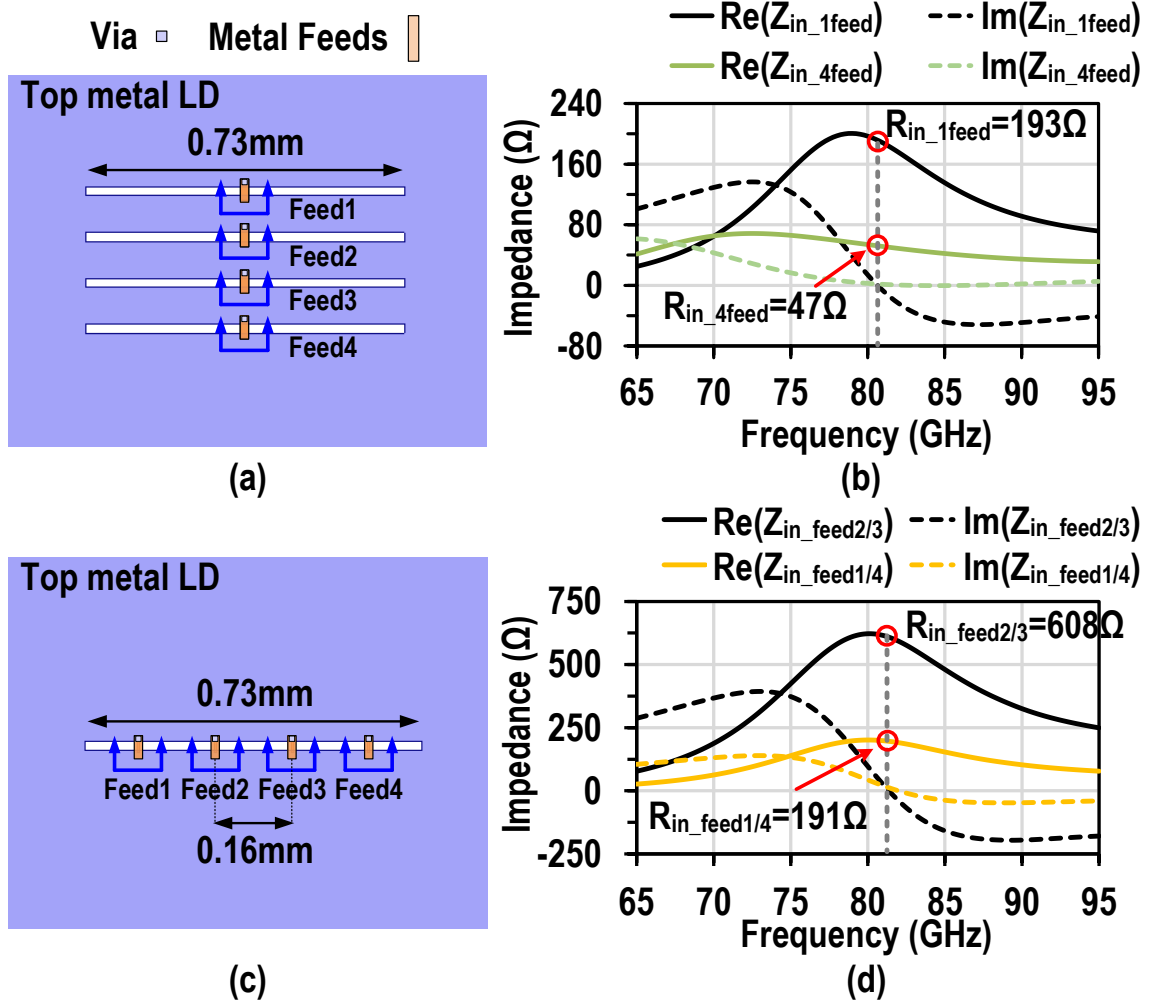


Figure 6-4 (a) EM model of the four near-field couple 0.5λ slot antennas, and (b) its antenna input impedance (R_{in_4feed} at resonance) compared with that of the conventional single-feed 0.5λ slot antenna (R_{in_1feed} at resonance). (c) EM model of the four-feed 0.5λ slot antenna, and (d) the antenna input impedance at the inner feed locations ($R_{in_feed2/3}$ at resonance) and at outer feed locations ($R_{in_feed1/4}$ at resonance).

In Figure 6-4c, four feeds are distributed with an equal separation (of 0.16mm) on a 0.5λ (0.73mm) slot dipole antenna, which is equivalent to parallel network configuration with impedance scaling. Knowing the exact location of each feed, we can calculate the on-antenna transformation ratios based on (6-2) as $k_i = \frac{1}{\sin[k(\frac{L}{2} - |x|)]}$, leading to $k_1 = k_4 = 1.95$, $k_2 = k_3 = 1.06$. Its equivalent circuit model is shown in Figure 6-3a with $R_{rad} = R_{in_1feed} = 193\Omega$ (EM simulated), and $k_1 = k_4 = 1.95$, $k_2 = k_3 = 1.06$. Assuming an equal power

combining case from all the paths, the input impedance at each antenna feed is simplified from (6-10) as

$$R_{in,i} = \frac{N \times R_{rad}}{k_i^2} \quad (6-14)$$

Substituting the values of N , R_{rad} , and k_{1-4} into (6-14), we can obtain $R_{in_feed1/4}$ and $R_{in_feed2/3}$ as 203Ω and 687Ω respectively, which matches well with the EM simulated values shown in Figure 6-4d, and demonstrates the equivalent parallel network connections among the feeds with impedance scaling.

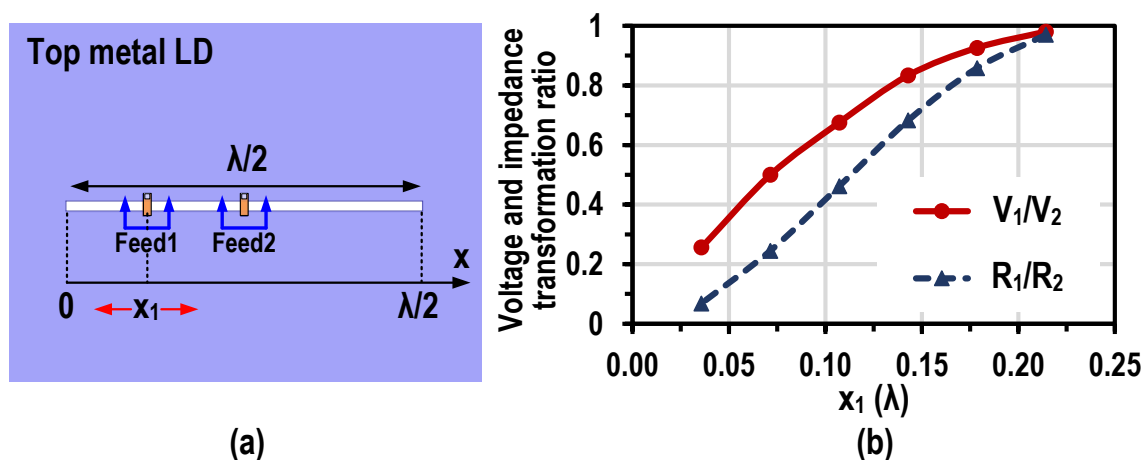


Figure 6-5 (a) EM model of the two-feed 0.5λ slot antenna with varying location of feed1 for voltage and impedance transformation. (b) Voltage and impedance transformation ratio between feed1 and feed2 when feed1 at different locations.

Besides series and parallel connections, multi-feed antennas can be designed to function as on-antenna passive transformers for impedance, voltage, and current scaling at each feed. In Figure 6-5a, a two-feed 0.5λ slot antenna is simulated with varying feed1 locations and fixed feed2 position. The voltage and impedance ratio between the two feeds (V_1/V_2 and R_1/R_2) are plotted in Figure 6-5b. A voltage transformation behavior with

impedance scaling is realized between the two antenna feed terminals, with the transformation ratios controlled by the relative locations of the two antenna feeds.

The dependence of the antenna input impedance on the location of antenna ports can thus be leveraged to facilitate a better antenna-circuit interface/matching network with a preferable impedance level for different applications. In antenna-TX co-designs, the antenna feeding location can be chosen to realize a resulting impedance down-scaling effect (as the feed moving away from the center in the example shown in Figure 6-5). Therefore, this reduces the required impedance transformation ratio for the output matching network of a PA that usually requires a low load impedance for high power delivery, which often improves both the passive loss and bandwidth. In antenna-RX co-designs, such dependence can also be utilized to provide closer noise or power matching. In summary, the locations of antenna ports are determined for desired antenna impedances or equivalent voltage (or current or impedance) transformation among the antenna ports.

6.2.4 Modelling Multi-Feed Antenna Networks as On-Antenna Hybrid Series and Parallel Connections with Scaling

Moreover, hybrid series and parallel connections through multi-feed antennas are also feasible. The derivation process of the implemented multi-feed antenna network is depicted in Figure 6-6, realizing various antenna-level signal conditioning capabilities (power splitting, voltage transformation, noise canceling, and gm-boosting), which will be further explained in Section 6.3. The folded slot antenna is chosen for its lower input impedance, and its conventional single-feed configuration simply behaves as a radiation resistance at its resonance (Figure 6-6a). By adding another feed on the same slot, a parallel network connection is formed directly on the antenna between the two feeds, with the feeding location determining the equivalent voltage transformation ratio (Figure 6-6b). In

addition, two near-field coupled slot antennas behave as one series network configuration (Figure 6-6c). Furthermore, for two near-field coupled antennas, extra antenna feeds $\pm VG$ tapped out of the high standing-wave voltage locations realize the desired passive feedforward voltage gain. Eventually, six feeds are implemented on a pair of near-field coupled folded slot antenna, with its half-circuit equivalent model shown in Figure 6-6d.

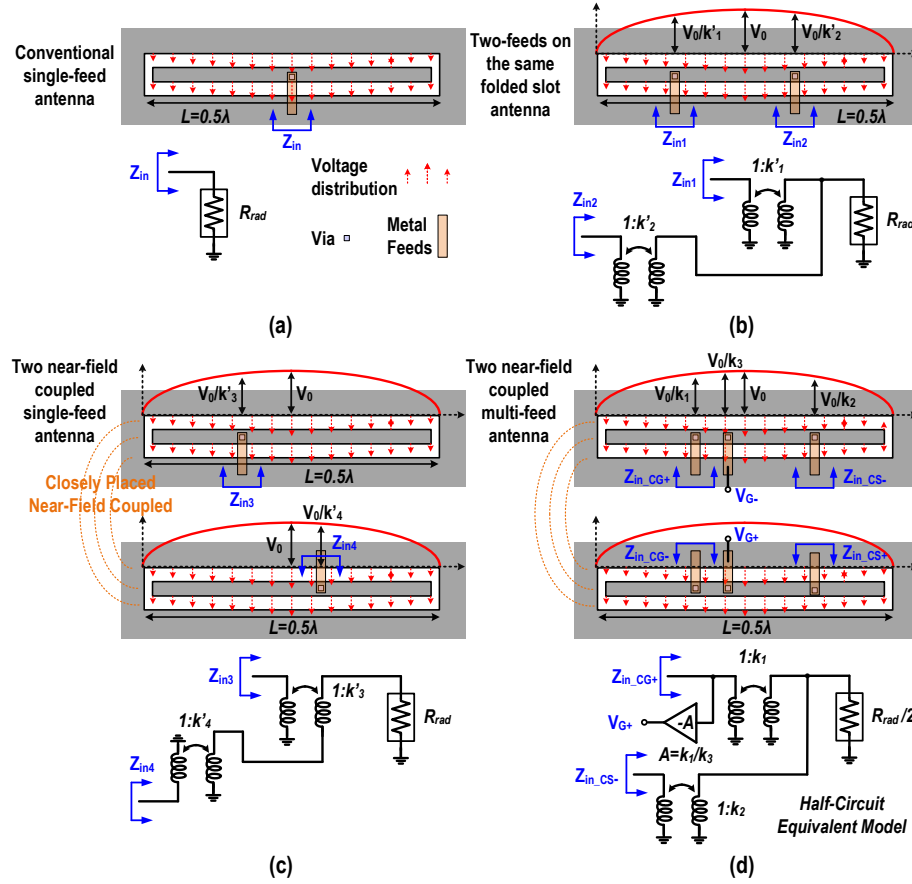


Figure 6-6 The derivation process of the eventually implemented multi-feed antenna network, starting from (a) the conventional single-feed case, to the addition of (b) the parallel and (c) the series power combining/splitting with an extra feed, and (d) the finally employed multi-feed antenna structure.

In summary, with the generic circuit models proposed in Section 6.2, designers can quickly derive the circuit equivalence of a given multi-feed antenna network. In turn, with a target passive circuit network, one can synthesize a multi-feed antenna structure to achieve the required on-antenna signal processing operations.

6.3 Multi-Feed Antenna and LNA Co-Design with On-Antenna Noise-Canceling and Gm-Boosting

6.3.1 On-Antenna Noise-Cancelling

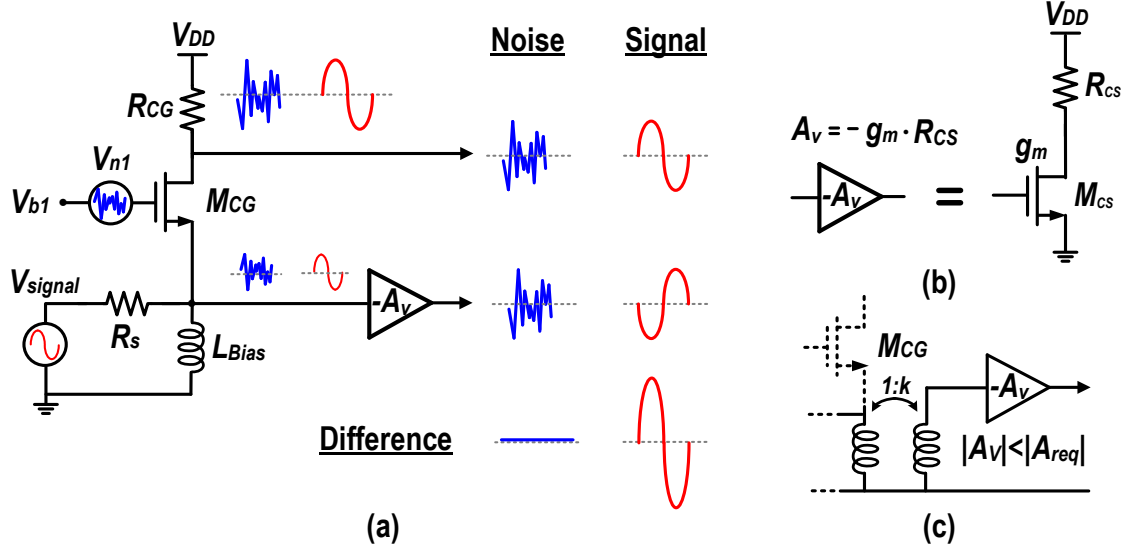


Figure 6-7 (a) Conventional electronics-only noise-canceling LNA topology. (b) CS amplifier commonly implemented as the required voltage amplifier. (c) A transformer utilized to realize voltage gain at zero power consumption.

The conventional noise-canceling low-noise amplifier (LNA) architecture [89] is depicted in Figure 6-7a. The common-gate (CG) amplifier provides input matching, while a voltage amplification stage replicates the CG device (M_{CG}) noise for noise cancellation at the differential output. Since the signal appears with same polarities at the source and drain nodes of M_{CG} , as opposed to the noise of M_{CG} with opposite polarities at the same two nodes, the signal is effectively amplified at the output. Often a common-source (CS) amplifier is implemented as the voltage amplifier (Figure 6-7b), with preferably a large transconductance (g_m) for a better overall NF [90], [91]. Since the device g_m is often limited by biasing and power consumption constraints, a transformer can be employed to realize passive voltage gain before the CS amplifier. However, at high mm-Wave frequencies, on-

chip transformer designs are constrained by parasitics, resulting in mostly 1:1 turn ratios, and thus a compromised passive voltage gain, as well as a reduced self-resonant frequency (SRF). In addition, the decreased input impedance of the CS stage provides undesirable loading to the input network and worsens input matching. Moreover, the increased transformer loss and CS-stage NF further degrade the overall noise performance.

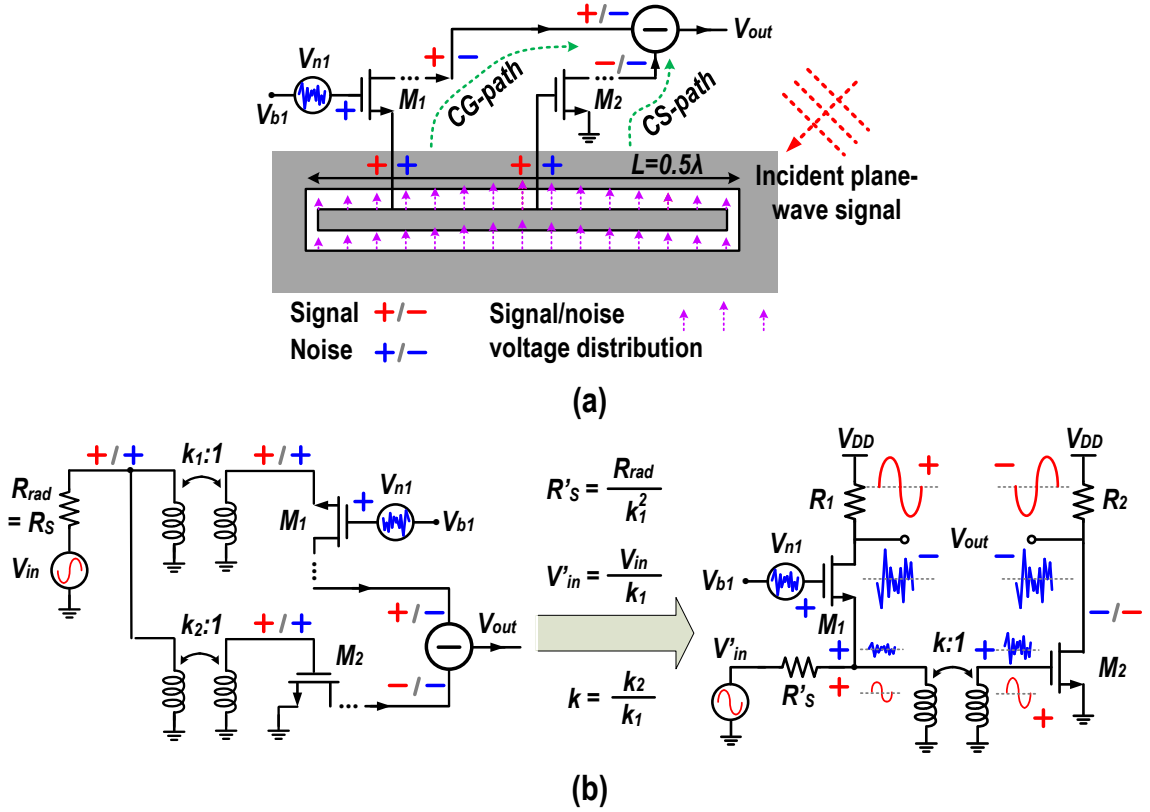


Figure 6-8 (a) On-antenna noise-canceling, and (b) its equivalent circuit model.

To address these challenges, we propose an on-antenna noise-canceling LNA topology by leveraging an on-chip multi-feed 0.5λ folded slot antenna (Figure 6-8a), with one antenna feed connected to the CG-path, and the other one feeding the CS-path for noise cancellation. At resonance, the folded slot antenna supports a standing-wave voltage distribution and thus behaves as a passive transformer (Section 6.2.2). Moreover, adjusting the feeding points alters the equivalent transformation ratios. It is worth noting that the CG input is at a lower standing-wave voltage location, while the CS input is selected to

interface with higher standing-wave voltage. On one hand, the antenna input impedance is lower at the lower voltage location, which facilitates the input matching of the CG stage. In parallel, with the offset locations of the two feeds, the equivalent on-antenna transformer realizes a passive voltage gain (from CG input to CS input) and reduce the required gm of the CS stage, with no additional loss, parasitics, and area, similar to the existing noise-canceling LNA in Figure 6-7c.

From the signal perspective, the incident plane-wave signal excites the standing-wave voltage pattern across the folded slot antenna, resulting in the same signal polarity at the input of CG and CS stage (marked in red in Figure 6-8a). The signal maintains its polarity at the CG output, while the CS amplifier flips its input signal polarity at output, leading to opposite signal polarities at the CG/CS outputs. Taking the differential outputs will thus amplify the desired signal.

From the noise perspective, the noise coming out of the CG amplifier exhibits different polarities at its source and drain nodes (marked in blue in Figure 6-8a). The noise at the source terminal further drives the antenna, exciting an identical standing-wave noise-voltage distribution across the slot, and thus leading to the same noise polarity at the input of the CS stage. After going through the CS path, the noise's polarity changes. Eventually, the noise polarities are the same at the CG/CS outputs. As a result, the noise (from the CG amplifier) is canceled at the differential output. Figure 6-8 depicts the antenna-circuit co-design schematic and the pure circuit model and clearly illustrates their similarities and correspondence.

6.3.2 On-Antenna G_m -Boosting

High mm-Wave RXs often use cascaded stages to increase power gain. Since only the 1st-stage CG amplifier noise is canceled, the gain of the 1st-stage LNA should be sufficiently large to suppress the noise of the following stages. Conventionally, cross-

coupled capacitors and multi-coil transformers are used to realize device g_m -boosting for CG amplifiers by providing feed-forward negative voltage gain between the source and gate nodes. However, these approaches introduce additional loss, parasitics, and area especially at high mm-Wave frequencies.

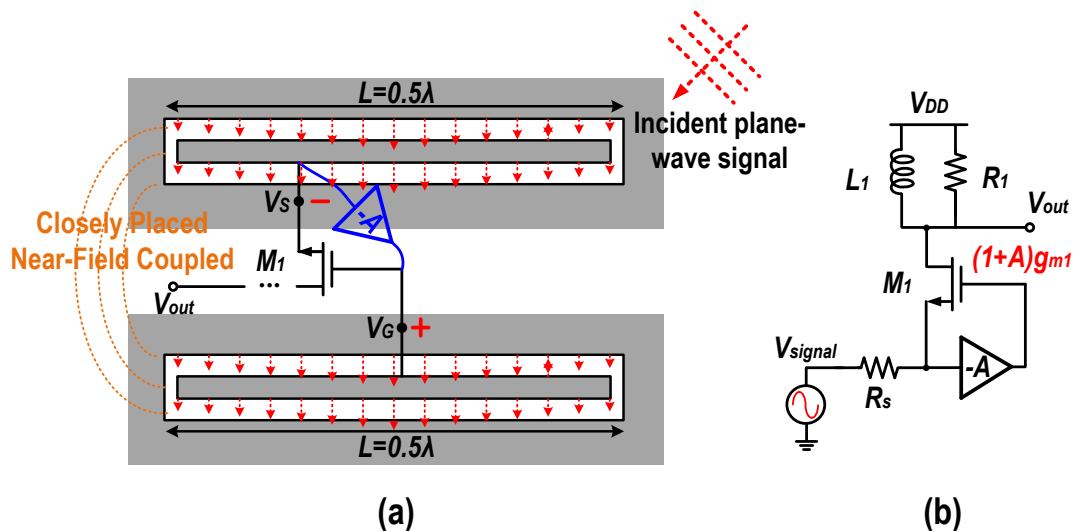


Figure 6-9 (a) On-antenna g_m -boosting, and (b) its equivalent circuit model.

To address the challenge, we propose an on-antenna g_m -boosting scheme (Figure 6-9a). For a pair of near-field coupled folded slot antennas, the opposite signal polarities between the top and bottom slots inherently provide the required negative feedforward gain (Section 6.2.1). Moreover, by tapping out the gate/source voltages (V_G or V_S) from the high/low standing-wave voltage locations, a passive voltage gain A is synthesized between the source and gate terminals as an on-antenna transformer. Changing the relative locations of the two feeds also change the voltage transformation ratio, i.e. the passive voltage gain, based on (6-2). The equivalent circuit model is shown in Figure 6-9b. As a result, the g_m of the CG transistor is boosted by a factor of $(1+A)$, suppressing the noise from the following stages. Again, the similarities and correspondence between the antenna-circuit co-design schematic and the pure circuit model are clearly depicted.

6.4 Design Details of the Antenna-LNA Front-End

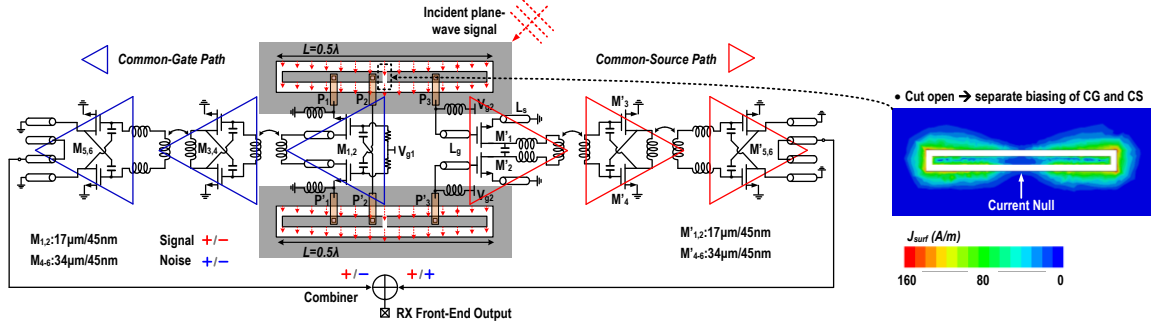


Figure 6-10 The top-level circuit schematic of the antenna-LNA front-end with on-antenna noise canceling and gm-boosting, and the EM-simulated surface current distribution (J_{surf}) of the on-chip multi-feed antenna at 80GHz.

Figure 6-10 illustrates the top-level circuit schematic including one gm-boosted CG path and one CS path that together cancel the noise from the 1st-stage CG amplifier. The CG path consists of a g_m -boosted CG amplifier following by two capacitive neutralized CS amplifiers, while an inductively degenerated CS amplifier with the same 2nd/3rd CS stages forms the CS path. The EM-simulated current-distribution of the proposed multi-feed antenna at 80GHz is plotted in Figure 6-10. The length of the antenna is 0.5λ , forming a current null at the center of the folded slot. As a result, its middle section of the antenna is cut open to allow different CG/CS biasing voltages, without affecting the antenna characteristics [86]. A comparison between the antenna radiation patterns and input impedances with and without the center-cut is shown in Figure 6-11. Note that this center-cut does not affect the on-antenna current distribution or far-field pattern, as well as impedance behaviors. The CS amplifiers with capacitor neutralization are employed for its enhanced differential-mode gain and stability. Transformers are used as the inter-stage matching network, with its center-taps properly terminated to ensure common-mode stability. Coupler-based baluns are implemented at the outputs of both paths with flipped polarity for noise cancellation after path combining.

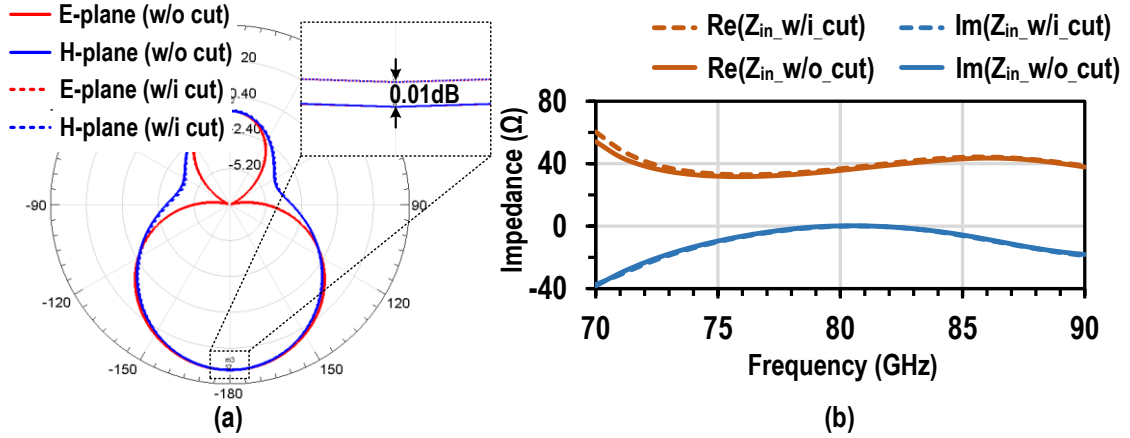


Figure 6-11 (a) A comparison between the antenna radiation patterns with and without the center-cut. **(b)** A comparison between the antenna input impedance with and without the center-cut.

6.4.1 Design Analysis for Signal Receiving

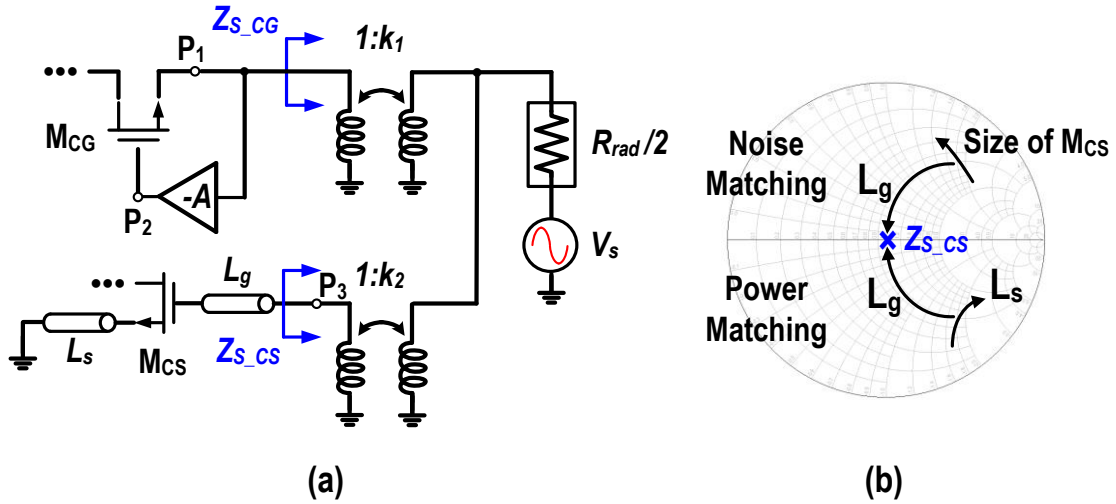


Figure 6-12 (a) The equivalent half-circuit model of the antenna-LNA front-end when receiving signals, and **(b)** the design trajectory on Smith-Chart for the simultaneous noise and power matching for the CS amplifier.

When receiving signals, the antenna-LNA front-end is equivalent to the half-circuit model shown in Figure 6-12a. The CG/CS stages are respectively matched to their source impedances $Z_{s,CG}$ and $Z_{s,CS}$, which are given by

$$Z_{s_CG} = R_{rad}/k_1^2 \quad (6-15)$$

$$Z_{s_CS} = R_{rad}/k_2^2 \quad (6-16)$$

where k_1 and k_2 are determined by the antenna feed locations. For the CG amplifier, the conjugate input impedance matching should be satisfied with the g_m -boosted device input impedance matched to the source impedance Z_{s_CG} , leading to

$$\frac{1}{g_{m_CG} \times (1 + A)} = \frac{R_{rad}}{k_1^2}. \quad (6-17)$$

For the CS amplifier, simultaneous noise and power matching is employed with the source and drain inductor (L_S and L_g) to minimize its noise contribution. The design trajectory is illustrated on the Smith Chart (Figure 6-12b). The size of the CS device (M_{CS}) is properly chosen to set the real part of the optimum noise impedance to match the source impedance (Z_{s_CS}). The input resistance of the device can also be transformed to Z_{s_CS} with the inductive source degeneration (L_S) according to $r_g + \omega_T L_S$, where r_g is the gate resistance, and ω_T is the device unity gain frequency. The gate inductor (L_g) further provides the reactive part of the input matching with $\omega_0(L_g + L_S) = (\omega_0 C_{gs})^{-1}$, achieving noise matching at the same time.

Through 3D EM simulation, the full communication link is demonstrated with the antenna-LNA front-end as the target RX and a dipole at the far-field as the TX (Figure 6-13a). To quantify RX power gain and linearity, the TX dipole is driven by a matched signal source, and the RX near-field coupled folded slot antennas are connected to the corresponding CG/CS inputs. Within the 3dB gain bandwidth, the RX input 1dB compression point (IP_{1dB}) is from -8 to -5.7dBm (Figure 6-13b). The frequency response

of the gain and IP_{1dB} is further summarized in Figure 6-13c, achieving wideband performance.

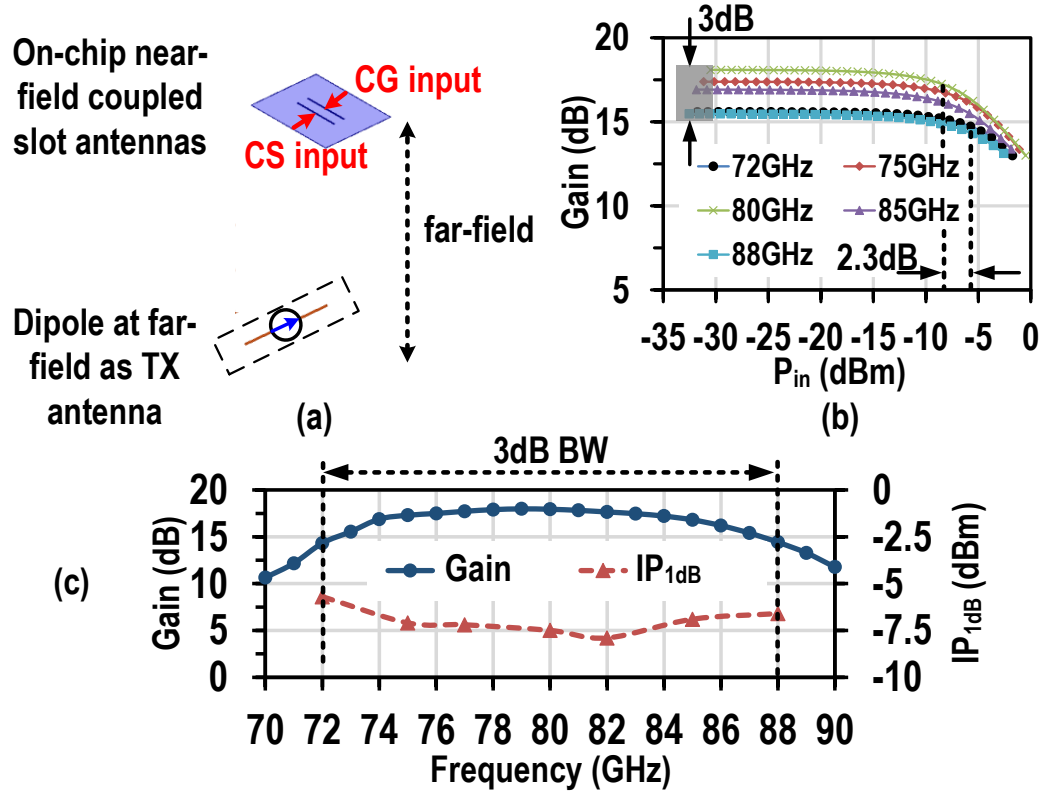


Figure 6-13 (a) The full-wave 3D EM simulation environment for radiation-based gain and linearity characterization. (b) Simulated gain compression at different frequencies. (c) Simulated frequency response of the gain and IP_{1dB} .

6.4.2 Design Analysis for Noise Cancellation

Interestingly, a different equivalent circuit should be used in the noise analysis (Figure 6-14), since the antenna is now driven by the 1st-stage CG amplifier noise source (V_n) and is further loaded by the input impedance of the CS stage (R_{rad}/k_{22}). As a result, the source impedance for the CG amplifier is now changed to

$$Z'_{s_{CG}} = R_{rad}/3k_1^2. \quad (6-18)$$

Consequently, the noise voltage V_X at the CG input can be calculated as

$$V_X = \frac{g_{m_CG} V_n Z'_{S_CG}}{1 + (1 + A) g_{m_CG} Z'_{S_CG}}. \quad (6-19)$$

We can further simplify the expression of V_X by substituting (6-17) and (6-18) into (6-19), as

$$V_X = \frac{V_n}{4(1 + A)} \quad (6-20)$$

Considering the effective transconductance of the CG and CS path (g'_{m_CG} and g'_{m_CS}), the noise current coming out of the CG and CS path can thus be derived as

$$i_{n_CG} = g'_{m_CG} [V_n - (1 + A)V_X], \text{ and} \quad (6-21)$$

$$i_{n_CS} = g'_{m_CS} \left(\frac{k_1}{k_2} \right) V_X. \quad (6-22)$$

respectively. To ensure noise current cancellation, i_{n_CG} and i_{n_CS} are designed to be equal ($i_{n_CG} = i_{n_CS}$), leading to

$$g'_{m_CG} = \frac{k_1}{k_2} \frac{1}{3(1 + A)} g'_{m_CS} \quad (6-23)$$

By equalizing the two noise currents, they will be effectively canceled when the difference is taken at the output. The noise cancellation bandwidth is ultimately limited by the antenna. The noise-canceling LNA is fundamentally a compelling technique to achieve broadband low noise performance (e.g. DC to GHz in the conventional designs), the statement is true under the assumption that a broadband source impedance (i.e. 50Ω) is

presented to the input of the LNA. In practice, all the antennas are frequency limiting structures. Going beyond the normal operation frequency range, the antenna will exhibit mismatched impedance from the desired in-band value, which will limit the noise cancellation performance. That being said, within the antenna bandwidth, our proposed on-antenna noise canceling technique does not compromise the noise-cancellation bandwidth compared to the conventional noise canceling structure, because identical noise canceling mechanism is realized with the input passive network synthesized by a multi-feed antenna. On the other hand, wideband antennas can be employed to extend the antenna impedance bandwidth. The above equivalent circuit models and equations serve as the theoretical guidelines for the implementation of the antenna-LNA front-end achieving on-antenna noise canceling and g_m -boosting.

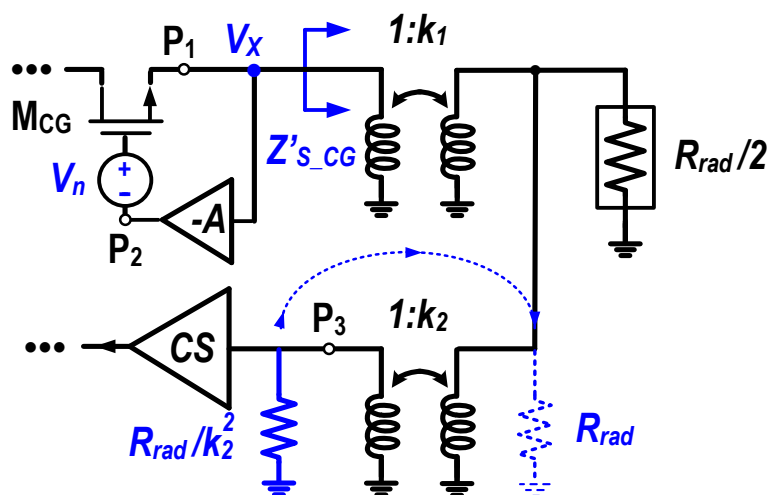


Figure 6-14 The equivalent half-circuit model of the antenna-LNA front-end in noise analysis.

The on-chip antenna achieves 70% radiation efficiency at 80GHz (Figure 6-15), benefiting from the high-resistivity substrate. The value will be later used to calculate the effective noise source temperature in the NF measurement. The simulated NF of the on-antenna noise-canceling LNA is plotted in Figure 6-15, with its CG-path separately simulated as a baseline E-band LNA design. The NF comparison is also shown in Figure 6-15. A substantial in-band NF improvement of 1.3dB at 80GHz verifies the proposed on-

antenna noise-canceling. Since the multi-feed LNA interfaces with frequency-dependent antenna source impedances, mismatch between $i_{n_{CG}}$ and $i_{n_{CS}}$ occurs and the CS noise matching degrades when deviating from the center frequency. Consequently, its NF degrades faster at the higher frequency range compared to a CG baseline LNA with a broadband source impedance. To further demonstrate the cancellation of the CG-stage noise, the noise contribution from different noise sources are simulated and summarized in Figure 6-16, showing that the noise contribution from the 1st-CG stage of the noise-canceling LNA is effectively reduced in-band.

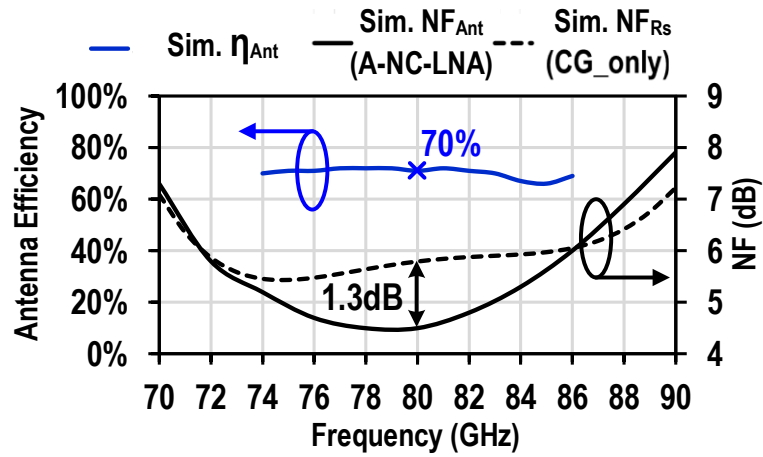


Figure 6-15 Simulated antenna efficiency, NF of the proposed on-antenna noise-canceling LNA (A-NC-LNA), and NF of the CG-only baseline LNA design.

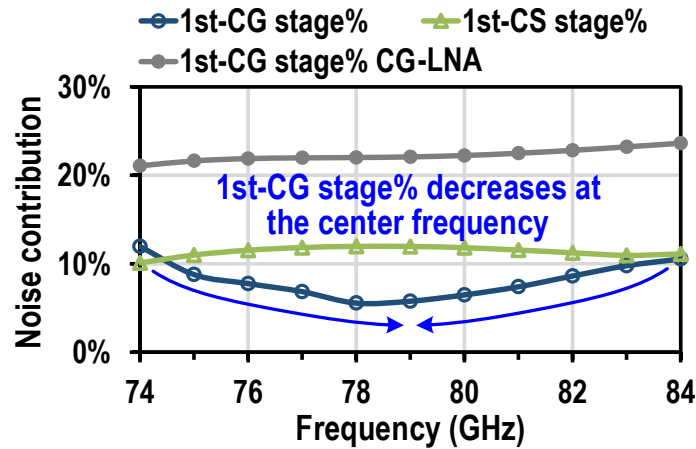


Figure 6-16 Simulated noise contributions of the 1st CG stage (1st-CG stage%) and the 1st CS stage (1st-CS stage%) of the noise-canceling LNA (NC-LNA), and of the 1st CG stage of the baseline CG-only LNA (1st-CG stage% CG-LNA).

6.5 Measurement Results

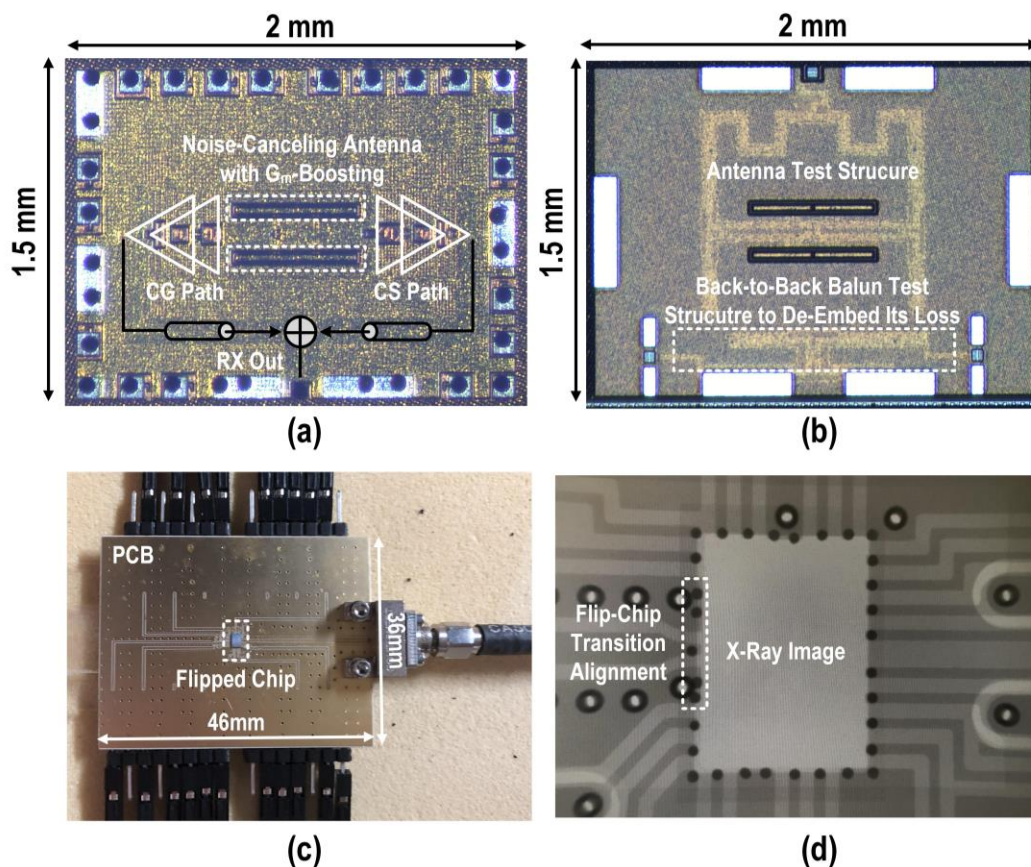


Figure 6-17 Die photographs of (a) the antenna-LNA front-end, and (b) antenna-only test structure. (c) Picture of the fully packaged module. (d) X-ray image for verification of the flip-chip transition alignment.

The E-band antenna-LNA front-end is fabricated in the GlobalFoundries 45nm CMOS SOI process (Figure 6-17a). A separate antenna test structure is also implemented to measure the antenna gain (Figure 6-17b). The die is in-house flip-chip packaged onto a Rogers high-frequency laminate (Figure 6-17c). X-ray is further performed to check the transition alignment (Figure 6-17d). This section presents the measurement results of both the Continuous-Wave (CW) and over-the-air modulation testing performance of the E-band antenna-LNA front-end.

6.5.1 Continuous-Wave Measurement

Due to the high mm-Wave operation frequency and the built-in antenna-load, two different methods are used to accurately measure the NF of the antenna-LNA front-end. First, the NF is obtained from the measured sensitivity of the RX with external down-conversion (Figure 6-18a) [12], [92], [93]. The conversion gain (CG) is obtained from the measured IF output power (P_{out}) at 600MHz and the RX received power (P_{rec_RX}), with the antenna test structure for antenna gain de-embedding. Therefore, the single-sideband CG can be expressed as

$$\begin{aligned} CG (dB) &= IF P_{out} (dBm) - P_{rec_RX} (dBm) \\ &= IF P_{out} (dBm) - [P_{out_TX} (dBm) + G_{TX_ant} (dB) \\ &\quad - Path Loss (dB) + G_{RX_ant} (dB)] \end{aligned} \quad (6-24)$$

where P_{out_TX} is TX output power, G_{TX_ant} and G_{RX_ant} are the TX and RX antenna gain. The single-sideband RX NF is then determined from the measured IF output noise floor, following

$$NF(dB) = IF \text{ noise floor} \left(\frac{dBm}{Hz} \right) + 174 \left(\frac{dBm}{Hz} \right) - CG(dB). \quad (6-25)$$

Cascaded NF equation is further used to de-embed the NF of the external down-conversion chain. Alternatively, a true Y-Factor radiation method is used to measure the NF (Figure 6-18b) [94]. The (effective input) noise temperature T_n is defined as

$$T_n = T_0(F - 1) \quad (6-26)$$

where $T_0 = 290K$, and F is the noise factor. Hot and cold noise inputs are generated using physical blackbody radiation noise sources presented to the antenna-LNA front-end input. With switching the hot/cold radiation noise sources, the output noise power ratio (Y-factor) is then measured. In this measurement, metal-backed absorbers at room temperature are used as the hot noise source with $T_h = T_0 = 290K$, while the same absorbers merged into

liquid nitrogen (LN₂) held in an EPS-foam bucket serve as the cold noise source with $T_c = 77\text{K}$. The hot/cold noise sources should be kept within the distance that ensures the emitted radiation from the noise sources is the only radiation observed by the main lobe of the RX antenna. It is also worth noting that the condensation formed on the surface of the foam bucket could scatter the emitted cold noise power. Therefore, a fan is used to prevent the buildup of condensation. Since the on-chip antenna radiates from both sides, the noise sources are placed on the top and bottom of the chip to cover the entire antenna radiation pattern. Due to the finite antenna efficiency, the equivalent noise source temperature T'_{src} is determined by [95]

$$T'_{src} = \eta_{Ant} T_{src} + (1 - \eta_{Ant}) T_0 \quad (6-27)$$

where η_{Ant} is the antenna efficiency and T_{src} is the noise source temperature (T_h or T_c). It not only consists of the actual noise source temperature T_{src} multiplied by a factor of η_{Ant} , but also includes the antenna thermal noise due to antenna loss. The Y-factor is the ratio of the noise output power with a hot noise source (N_{hot}) to that with a cold noise source (N_{cold}), which can be further derived as

$$\begin{aligned} Y &= \frac{N_{hot}}{N_{cold}} = \frac{k[\eta_{Ant} T_{src}^h + (1 - \eta_{Ant}) T_0] B G_{DUT} + k T_{DUT} B G_{DUT}}{k[\eta_{Ant} T_{src}^c + (1 - \eta_{Ant}) T_0] B G_{DUT} + k T_{DUT} B G_{DUT}} \\ &= \frac{\eta_{Ant} T_{src}^h + (1 - \eta_{Ant}) T_0 + T_{DUT}}{\eta_{Ant} T_{src}^c + (1 - \eta_{Ant}) T_0 + T_{DUT}} \end{aligned} \quad (6-28)$$

where k is Boltzmann's constant. B is the measurement bandwidth. G_{DUT} is the gain of the device under test (DUT). T_{DUT} is the DUT noise temperature to be measured. To reflect the device noise performance, the measured double-sideband NFs using the two methods are plotted in Figure 6-18c. With the simulated 70% η_{Ant} , we notice there is a discrepancy in the measured NF between the two methods. It is possibly due to a lower η_{Ant} of the actual

antenna implementation. Assuming a 60% η_{Ant} , the two approaches achieve a closer agreement on the measured NF. The measured power gain is 16.8dB at 79GHz, with a 3dB bandwidth from 73-88GHz (Figure 6-18c).

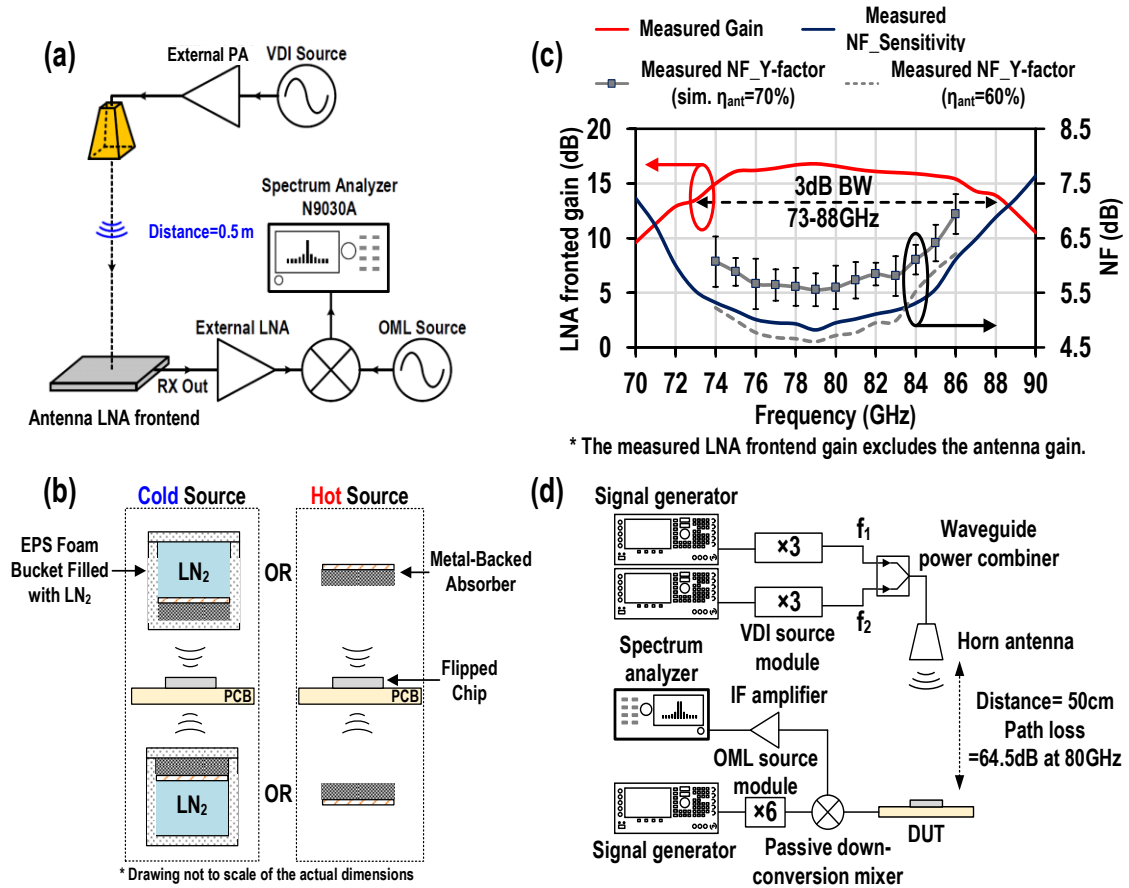


Figure 6-18 (a) RX CG measurement setup. (b) NF measurement setup with true Y-factor radiation method. (c) Measured gain and NF of the DUT. (d) Far-field radiation IIP3 measurement setup.

Due to the high path loss at E-band, i.e. 64.5dB at a distance of 0.5m at 80GHz, the transmitting power is not sufficient to saturate the RX. As a result, a far-field radiation-based IIP3 measurement is performed to characterize the linearity of the antenna-LNA front-end (Figure 6-18d). The two-tone signals are generated from the signal generators, multiplied, combined, and transmitted by the horn antenna. The signal is received by the DUT, down-converted, and sent to the spectrum analyzer for measurement. The two-tone testing results are plotted in Figure 6-19a, showing 0.5dBm measured IIP3 at 79GHz. The

measured IIP3 over the frequency is further summarized in Figure 6-19a. Moreover, the antenna radiation pattern is also measured and plotted in Figure 6-19b with simulation results.

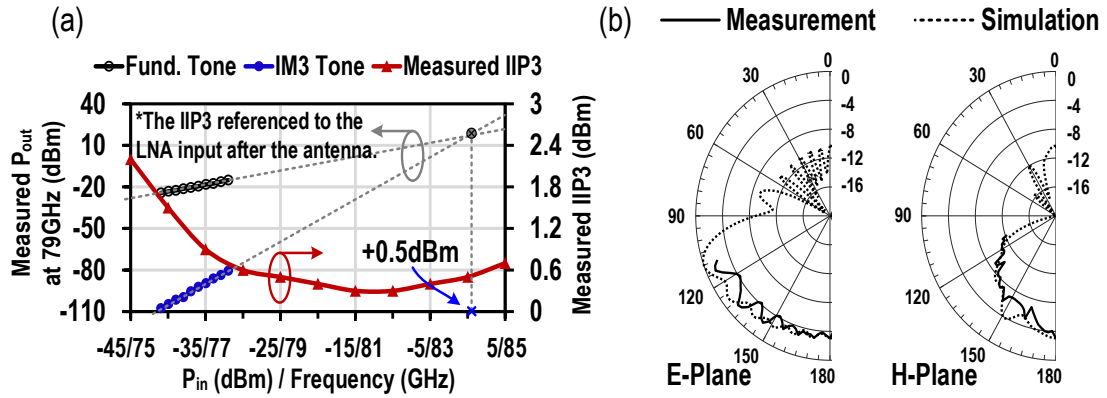


Figure 6-19 (a) Two-tone testing result at 79GHz, and IIP3 over frequencies. (b) Measured and simulated antenna radiation patterns at 79GHz.

6.5.2 Over-the-Air Modulation Measurements

An E-band wireless link is built to test the DUT performance with high-speed modulations (Figure 6-20a). The arbitrary waveform generator (AWG) generates the modulated signal that is then up-converted, amplified, and sent to horn antenna for transmission. The DUT receives the modulated signal that is then down-converted and relayed to the mixed-signal oscilloscope for digital demodulation. The wireless modulation testing results with 64-QAM at 12Gb/s and a maximum 16.5Gb/s are shown in Figure 6-20b, demonstrating the front-end ability to support high-fidelity wideband complex modulated signals. Additional modulation performance with different modulation schemes over the established 80GHz over-the-air channel is further summarized in Figure 6-20c, supporting >10Gb/s high-order QAM signals.

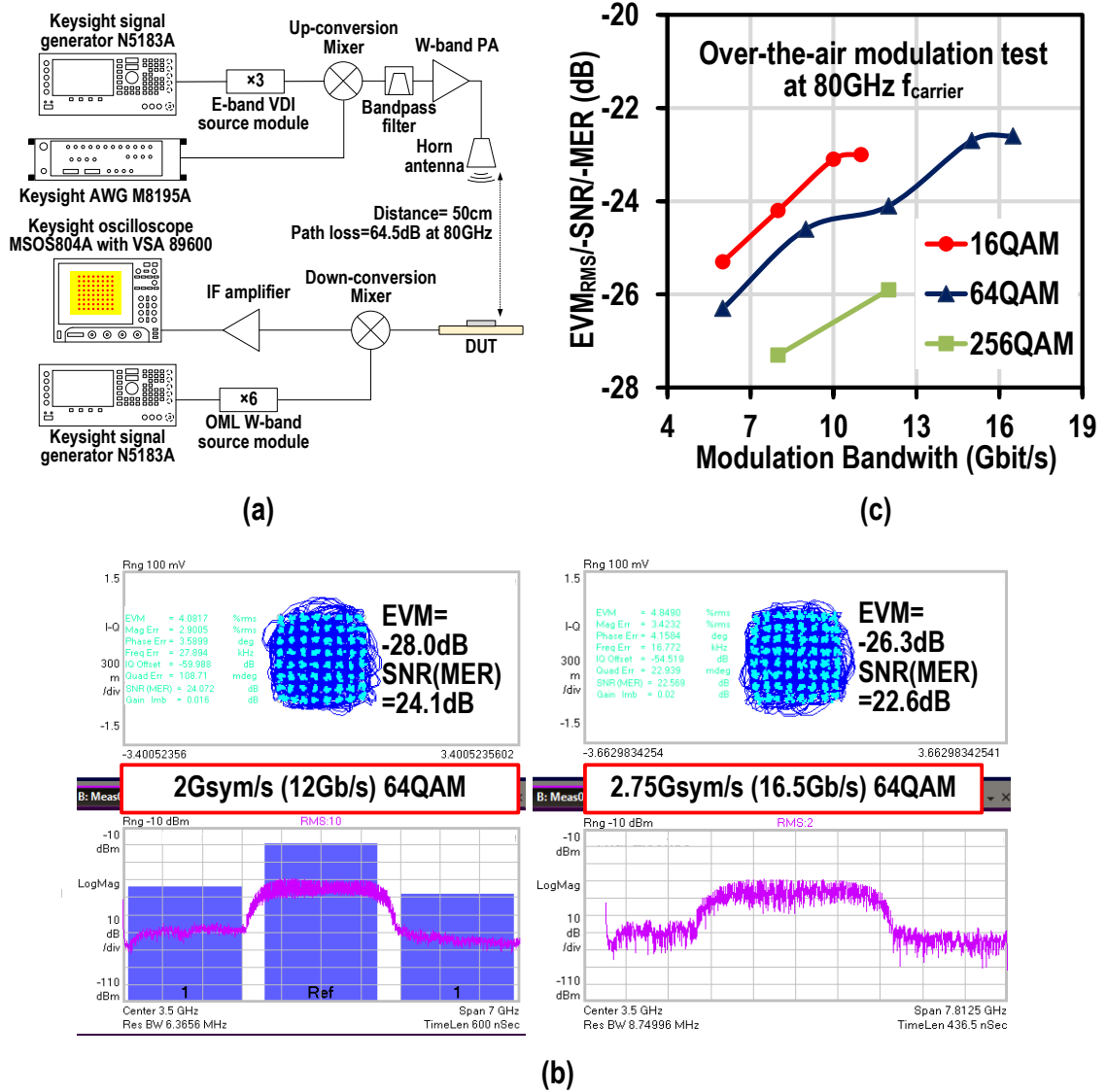


Figure 6-20 (a) The modulation testing setup. (b) Measured demodulated 64-QAM constellations and spectrum at 12Gb/s and 16.5Gb/s. (c) Over-the-air modulation testing results with different modulation schemes.

Table 6-1 compares this work with the state-of-the-art RX/LNA at E-band. Unlike the electronics-only LNA or RX designs that are all characterized and reported based on a broadband 50 Ω source impedance, the effect of the mismatch of antenna source impedance is captured by the antenna-LNA co-designed frontend performance over frequencies where the antenna impedance deviates from the desired/matched value at center frequency. Our

reported NF frequency response is therefore more practical and comprehensive for the actual wireless communication systems, since it takes the frequency dependent behavior of antenna impedance into account.

Adopting two different measurement methods, this work demonstrates a competitive NF at E-band. Two factors mainly contribute to the high linearity achieved in our proposed antenna-LNA front-end. First, the incoming signal power is equally split on-antenna into the CG and CS path, which extends the LNA linearity (e.g. P_{1dB}). Second, most state-of-the-art LNAs are single-ended implementations, while our proposed antenna-circuit co-design support a differential LNA implementation by offering effective input baluns for free through the antenna, which increases the LNA linearity by 3dB. As a result, the linearity of the proposed antenna-LNA front-end will be substantially improved beyond that of a conventional single-ended LNA. This is observed in the performance comparison table. The on-antenna power splitting further facilitates a high linearity implementation, showing the best reported input P_{1dB} and IIP3. Moreover, over the air modulation testing is first performed at E-band, supporting a maximum 16.5Gb/s 64-QAM signal. The Figure of Merit ($FoM = \frac{G}{F_{min}-1} \times \frac{IP_{1dB}}{P_{DC}}$) for RX/LNA is further used for performance comparison. This work shows the highest FoM among reported E-band RX/LNA designs in silicon.

At (high) mm-Wave frequencies, antenna arrays are essential in wireless communication to compensate for the high path loss and facilitate beamforming operation. Since the overall array NF in reality (with N channels) is relaxed by $10\log(N)$ in decibel, the linearity becomes more critical for receivers in an array, especially considering the scenarios of simultaneous reception of multiple streams (e.g. Multi-User MIMO) and presence of any strong interferers that can be co-side interferences. In these scenarios, a RX/LNA design with good linearity yet still competitive NF (as demonstrated by our proposed antenna-LNA front-end) will be very useful to support multi-stream MIMO

receiving and ensure tolerance of large interferers, while maintaining a good RX sensitivity [96].

Table 6-1 Comparison with State-of-The-Art E-band Silicon-Based LNAs/RXs

	Topology	3dB BW(GHz)	Load Termination	Power Gain(dB)	Noise Figure (dB)	IP _{1dB} (dBm)	IIP3(dBm)	OTA Measurement	Modulation Data Rate, Type, EVM	P _{DC} (mW)	Core Area (mm ²)	FoM [#]	Process
L. Gao RFIC'18	Inductively degenerated CS with gain boosting	74-99	Wideband 50Ω	12	4.2-5.7	-21	-11.4*	N.A.	Continuous Wave	4.7	0.42	0.0164	45nm CMOS SOI
L. Gao TMTT'20	Inductively degenerated Cascode with gain boosting	77(f ₀), 12(BW)	Wideband 50Ω	20	4.6 (min.)	-27.4	-17.8*	N.A.	Continuous Wave	9	0.15	0.0108	22nm CMOS
		77(f ₀), 13(BW)		24	4.6 (min.)	-26.8	-17.2*			16	0.15	0.0174	FD-SOI
		92(f ₀), 31(BW)		18.2	5.8 (min.)	-22.8	-13.2*			16	0.15	0.0077	
G. Feng JSSC'17	Pole-converging with xmfr feedback	63-93	Wideband 50Ω	18.5	5.5-7.9	-15	-5.4*	N.A.	Continuous Wave	27	0.24	0.0325	65nm CMOS
				13.3	6.4-8.5	-14	-4.4*			12		0.0210	
Y. Yu JSSC'17	Xmfr-based g _m -boosting and pole tuning	55-90	Wideband 50Ω	17.7	5.4-7.4	-15.4	-5.8*	N.A.	Continuous Wave	19	0.37	0.0362	65nm CMOS
M. Vigilante ISSCC'16	Xmfr-based g _m -boosted CG	68-96	Wideband 50Ω	29.6	6.4-8.2	-28.1	-18.5*	N.A.	Continuous Wave	31.3	0.255	0.0134	28nm CMOS
				18	7.8-9.8	-12.3	-2.7*			11.7		0.0631	
O. Inac TMTT'14	Inductively degenerated CS	76-88	Wideband 50Ω	14.7	5.7-8.3	-15.2	-5.6*	N.A.	Continuous Wave	13.5	N.A.	0.0243	45nm CMOS SOI
This work	On-antenna noise-canceling and g _m -boosting	73-88	Antenna Load	16.8	4.8-6.1 (Sensitivity) 5.6-6.9 (Y-factor, η _{ant} =70%) 4.6-6.2 (Y-factor, η _{ant} =60%)	-7.4* at 75GHz -9.2* at 80GHz -8.9* at 85GHz	2.2 at 75GHz 0.4 at 80GHz 0.7 at 85GHz	Yes	12/16.5Gb/s, 64QAM, -28/-26.3dB	46	0.63 (w/ on-chip antenna)	0.0937	45nm CMOS SOI

* The values are estimated from IIP3=IP_{1dB}+9.6dB. # FoM = $\frac{G}{F_{min}-1} \times \frac{IP_{1dB}}{P_{DC}}$

6.6 Conclusion

This paper presents a generic multi-feed antenna system that can be fundamentally categorized as series, parallel, and hybrid configurations. Moreover, multi-feed antennas can be designed to function as on-antenna passive transformers for impedance, voltage, and current scaling at each feed. To offer a circuit design intuition, equivalent circuit modeling is proposed to theoretically explain different antenna-level signal processing operations, which is further verified by full-wave EM simulations. As a proof-of-concept, we propose an E-band antenna-LNA front-end that realizes on-antenna noise canceling and gm-boosting. A true Y-factor radiation method is first introduced to measure the NF of the LNA/RX integrated with antenna. 4.8dB NF with 2.2dBm IIP3 is demonstrated in the CW measurement, showing the best reported LNA/RX FoM. Moreover, over-the-air modulation testing is performed on the DUT in an established 80GHz wireless channel, supporting >10Gb/s high-fidelity high-order QAM signals.

CHAPTER 7. CONCLUSION

In this dissertation, we discussed our approaches towards the development of fully integrated TRX front-end circuits for the next-generation energy-efficient, linear, and wideband wireless communication systems. Mm-wave spectra is leveraged in the designs to address the exponentially growing data-rate demand. CMOS technology offers a low-cost platform with powerful computation resources and a high level of integration. However, mm-Wave CMOS circuit performance is greatly limited by the low device breakdown voltage and cut-off frequency, compared with compound III-V processes. The lossy on-chip passive components further limit the achievable circuit performance in CMOS at mm-Wave. We have presented several new system architectures and circuit techniques to overcome these limitations and demonstrated the state-of-the-art circuit performance.

First, we propose a multi-feed antenna structure that synthesizes the desired far-field radiation characteristics with high-efficiency direct on-antenna power combining. The multiple antenna feeds are driven simultaneously, and the driving signals are scaled with proper amplitudes/phases which together actively synthesize the desired on-antenna RF current/voltage distribution, achieving the desired far-field radiation pattern. Compared to power combining using on-chip/on-package passive networks, the on-antenna power combining is much more efficient. It also provides the flexibility to optimize the antenna driving impedance based on the locations of the antenna feeds. Compared to spatial power combining using antenna arrays, it is capable of boosting the total radiated power in only one antenna footprint and maintaining the element beamwidth and the field-of-view as a conventional single-feed antenna. In addition, the multi-feed antennas can be implemented in an array fashion for further EIRP enhancement and to facilitate beamforming and MIMO operation.

Secondly, we took a step further to develop our proposed antenna-electronics co-design methodology by demonstrating on-antenna PA active load modulation beyond the earlier proved on-antenna power combining. We present a packaged 28-GHz Chireix outphasing transmitter for PA efficiency enhancement at both peak and back-off output power. The main objective is to investigate the possibility of employing a multi-feed antenna as a multi-port passive network to perform outphasing active load modulation. As a proof of concept, an outphasing TX architecture is proposed by leveraging a dual-feed loop antenna to achieve high efficiency transmission of wideband complex modulated signals. Theoretical analysis and simulation results prove that the proposed DLA is electrically equivalent to an ideal differential series non-isolating power combiner, enabling superior on-antenna outphasing operation. Multi-functional signal processing is therefore achieved in a single-loop antenna footprint, including high-efficiency on-antenna power combining, outphasing active load modulation, and mm-Wave signal radiation. Moreover, unlike conventional spatial vectorial combining techniques (e.g., spatial IQ or spatial outphasing), the antenna-level signal processing preserves the wide antenna unit field of view and is particularly suitable for array or MIMO applications. The proposed Chireix TX contains two phase-shifted sub-TXs simultaneously driving a DLA on package. The measurements demonstrate a 53%/43% PA drain/power added efficiency (DE/PAE) at 17.1-dBm P_{sat} and 36%/23% DE/PAE at 6-dB PBO. The high-efficiency Chireix TX supports up to 15 Gb/s 64-QAM with 10.4-dBm average output power and 34% average PA DE (19.2% average PAE) while maintaining EVM/ACLR better than -27.5 dBc/ -28 dBc in a wireless radiation testing environment.

Next, a wideband high-efficiency frequency doubler leveraging transistor multi-port waveform shaping is presented in Chapter 3. Unlike the conventional push-push pair with grounded source terminals, both the gates and sources of the proposed doubler are simultaneously driven by 180° out-of-phase signals. As a result, the drain current

bifurcation is greatly reduced, leading to suppression of the undesired 4th harmonic and significant enhancement of 2nd harmonic current. The EKV FET model is also adopted to mathematically analyze the current waveform shaping in both conventional and proposed topologies, which agrees well with the circuit simulations. Broadband fundamental matching and a dual-resonance 2nd harmonic trap filter together guarantee the wideband frequency doubling performance. Prototyped in 45nm CMOS-SOI, the proposed doubler achieves 25% peak drain efficiency, instantaneously covering 46-89GHz (64% fractional bandwidth).

In Chapter 4, the earlier demonstrated (on-antenna) voltage-mode outphasing architecture is further improved by proposing a new current-mode inverse outphasing architecture, which unlocks a high-performance outphasing implementation at (high) mm-Wave. We present a mm-wave transmitter front-end employing the new inverse outphasing architecture with current-mode PAs. Our study on the conventional outphasing operation reveals its strong dependence on its voltage-mode driving source assumption and thus exhibits major limitations at mm-wave, since efficient and linear mm-wave PAs often behave as current sources. To address this challenge, we propose a current-mode inverse outphasing architecture that employs current-mode driving source and is inherently compatible with mm-wave linear PAs. Moreover, the conventional series outphasing combiner is replaced by a much simpler and low-loss parallel power combining scheme. Closed-form mathematical expressions are derived for both the outphasing and inverse outphasing operations, including the active load modulation, Chireix compensations, and outphasing efficiency, which fundamentally explains the limitations of the conventional approach and the advantages of the inverse outphasing architecture. Further theoretical analysis discovers a circuit duality relationship between outphasing and inverse outphasing architectures, which offers circuit intuitions. As a proof-of-concept, we implement a 28GHz TX front-end using cascode PAs based on inverse outphasing architecture. In the

measurement, the TX achieves 22.7dBm P_{sat} with 42.6% PA drain efficiency. The TX exhibits 1.5 \times PA efficiency enhancement at 6dB PBO, validating the high-efficiency inverse outphasing active load modulation. Modulation tests with high-order QAM signals demonstrate that the TX supports >10Gb/s high-fidelity complex signals and achieves the state-of-the-art modulation performance.

Lastly, we further extend the antenna-electronics co-design concept to RX designs, proposing an E-band LNA co-designed and co-integrated with an on-chip multi-feed antenna for antenna-level LNA noise-canceling and gm-boosting. Different from conventional approaches that view antennas as a simple 50Ω radiation load, we exploit antennas as multi-feed passive radiating networks with direct on-antenna signal conditioning and processing capabilities. Such an antenna-electronics co-design concept can potentially advance wireless frontend performance beyond electronics-only designs and opens the door to a plethora of frontend innovations. We also propose equivalent circuits to model multi-feed antenna systems and elucidate on-antenna signal processing operations. As a proof of concept, we propose an antenna-LNA co-designed architecture and explore the interactions among a common-gate LNA path, a common-source LNA path, and a pair of near-field coupled folded slot antennas for on-antenna noise-cancellation and gm-boosting. In the measurements, a true Y-factor radiation method is introduced as a new approach to measure the NF of the on-chip multi-feed antenna and LNA/RX integration. Then, we perform the conventional sensitivity-based NF measurement. Both measurements show accurate and consistent NF characterization at high mm-Wave. The E-band antenna-LNA frontend is implemented in the Globalfoundries 45nm CMOS SOI process and demonstrates 4.8dB NF with 2.2dBm IIP3, achieving the best reported FoM at the similar frequencies. Furthermore, over-the-air modulation tests are demonstrated and support >10Gb/s high-fidelity high-order QAM signals over an E-band wireless link.

REFERENCES

- [1] S. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech House, 2006.
- [2] T. Chi, S. Li, J. S. Park, and H. Wang, "A multifeed antenna for high efficiency on-antenna power combining," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6937–6951, Dec. 2017.
- [3] S. Li, T. Chi, J. S. Park, and H. Wang, "A multi-feed antenna for antenna-level power combining," in *Proc. IEEE Int. Symp. Antennas Propag.*, Jun. 2016, pp. 1589–1590.
- [4] T. Chi *et al.*, "A 60 GHz on-chip linear radiator with single-element 27.9 dBm P_{sat} and 33.1 dBm peak EIRP using multifeed antenna for direct on-antenna power combining," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 296–297.
- [5] S. Li, T. Chi, Y. Wang, and H. Wang, "A millimeter-wave dual-feed square loop antenna for 5G communications," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6317–6328, Dec. 2017.
- [6] S. Yost. (Jun. 2016). mmWave: The battle of the bands. National Instruments Corp., Austin, TX, USA. [Online]. Available: <http://www.bi.com/white-paper/53096/en/#toc2>
- [7] A. I. Sulyman, A. Alwarafy, G. R. MacCartney, T. S. Rappaport, and A. Alsanie, "Directional radio propagation path loss models for millimeter-wave wireless networks in the 28-, 60-, and 73-GHz bands," *IEEE Trans. Wireless Commun.*, vol. 15, no. 10, pp. 6939–6947, Oct. 2016.
- [8] A. I. Sulyman, A. T. Nassar, M. K. Samimi, G. R. MacCartney, Jr., T. S. Rappaport, and A. Alsanie, "Radio propagation path loss models for 5G cellular networks in the 28 GHz and 38 GHz millimeter-wave bands," *IEEE Commun. Mag.*, vol. 52, no. 9, pp. 78–86, Sep. 2014.
- [9] G. R. MacCartney, T. S. Rappaport, S. Sun, and S. Deng, "Indoor office wideband millimeter-wave propagation measurements and channel models at 28 and 73 GHz for ultra-dense 5G wireless networks," *IEEE Access*, vol. 3, pp. 2388–2424, Dec. 2015.
- [10] T. S. Rappaport, G. R. MacCartney, Jr., M. K. Samimi, and S. Sun, "Wideband millimeter-wave propagation measurements and channel models for future wireless communication system design (invited paper)," *IEEE Trans. Commun.*, vol. 63, no. 9, pp. 3029–3056, Sep. 2015.

- [11] S. Li, T. Chi, J. Park, W. Khan, H. Wang, and J. Papapolymerou, "A fully packaged D-band MIMO transmitter using high-density flipchip interconnects on LCP substrate," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, Sep. 2016, pp. 1–4.
- [12] T. Chi, M. Huang, S. Li, and H. Wang, "A packaged 90-to-300 GHz transmitter and 115-to-325 GHz coherent receiver in CMOS for fullband continuous-wave mm-wave hyperspectral imaging," in *ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 304–305.
- [13] C. Balanis, *Antenna Theory: Analysis and Design*, 3rd Edition, New York: J. Wiley & Sons, 2005.
- [14] W. Stutzman and G. Thiele, *Antenna Theory and Design*, 3rd ed. New York, NY, USA: Wiley, 2012.
- [15] K. Datta and H. Hashemi, "Performance limits, design and implementation of mm-wave SiGe HBT class-E and stacked class-E power amplifiers," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2150–2171, Oct. 2014.
- [16] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Distributed active transformer—A new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.
- [17] J. X. Yun and R. G. Vaughan, "Open slot antenna in a small ground plane," *IET Microw. Antennas Propag.*, vol. 5, no. 2, pp. 200–213, 2011.
- [18] D. C. Thompson, O. Tantot, H. Jallageas, G. E. Ponchak, M. M. Tentzeris, and J. Papapolymerou, "Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 4, pp. 1343–1352, Apr. 2004.
- [19] A. L. Vera-López, S. K. Bhattacharya, C. A. Donado-Morcillo, J. Papapolymerou, D. Choudhury, and A. Horn, "Novel low loss thin film materials for wireless 60 GHz application," in *Proc. 60th IEEE Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2010, pp. 1990–1995.
- [20] S. Li, M. Yi, S. Pavlidis, H. Yu, M. Swaminathan, and J. Papapolymerou, "Investigation of surface roughness effects for D-band SIW transmission lines on LCP substrate," in *Proc. IEEE Radio Wireless Symp.*, Phoenix, AZ, USA, Mar. 2017, pp. 121–124.
- [21] M. Yi, S. Li, H. Yu, W. Khan, C. Ulusoy, A. Lopez, J. Papapolymerou, M. Swaminathan, "Surface Roughness Modeling of Substrate Integrated Waveguide in D-Band," *IEEE Trans. Microw. Theory. Tech.*, vol. 64, no. 4, pp. 1209–1216, Apr. 2016.

- [22] S. Hu, F. Wang, and H. Wang, "A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 32–34.
- [23] M. Özen, N. Rostomyan, K. Aufinger, and C. Fager, "Efficient millimeter wave Doherty PA design based on a low-loss combiner synthesis technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1143–1145, Dec. 2017.
- [24] P. Indirayanti and P. Reynaert, "A 32 GHz 20 dBm-PSAT transformerbased Doherty power amplifier for multi-Gb/s 5G applications in 28 nm bulk CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 45–48.
- [25] N. Rostomyan, M. Özen, and P. Asbeck, "28 GHz Doherty amplifier in CMOS SOI with 28% back-off PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 446–448, May 2018.
- [26] H. T. Nguyen, T. Chi, S. Li, and H. Wang, "A 62-to-68GHz linear 6Gb/s 64QAM CMOS Doherty radiator with 27.5%/20.1% PAE at peak/6dB back-off output power leveraging high-efficiency multi-feed antenna-based active load modulation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 402–403.
- [27] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
- [28] F. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. COM-33, no. 10, pp. 1094–1099, Oct. 1985.
- [29] S. Moloudi and A. A. Abidi, "The outphasing RF power amplifier: A comprehensive analysis and a class-B CMOS realization," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013.
- [30] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 6, pp. 2129–2138, Jun. 2005.
- [31] D. Zhao, S. Kulkarni, and P. Reynaert, "A 60-GHz outphasing transmitter in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3145–3183, Dec. 2012.
- [32] P. Godoy, S. Chung, T. Barton, D. Perreault, and J. Dawson, "A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2372–2384, Oct. 2012.
- [33] T. Barton, "Not just a phase: Outphasing power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 18–31, Feb. 2016.

- [34] L. C. N. de Vreede *et al.*, “Outphasing transmitters, enabling digital-like amplifier operation with high efficiency and spectral purity,” *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 216–225, Apr. 2015.
- [35] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, “A flip-chip-packaged 25.3 dBm class-D outphasing power amplifier in 32 nm CMOS for WLAN application,” *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, Jul. 2011.
- [36] B. Rabet and J. Buckwalter, “A high-efficiency 28 GHz outphasing PA with 23 dBm output power using a triaxial balun combiner,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 174–176.
- [37] S. Li, T. Chi, H. T. Nguyen, T.-Y. Huang, and H. Wang, “A 28GHz packaged Chireix transmitter with direct on-antenna outphasing load modulation achieving 56%/38% PA efficiency at peak/6dB back-off output power,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 68–71.
- [38] J. H. Qureshi *et al.*, “A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning,” *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 1925–1935, Aug. 2009.
- [39] Z. Hu, L. C. N. de Vreede, M. S. Alavi, D. A. Calvillo-Cortes, R. B. Staszewski, and S. He, “A 5.9 GHz RFDAC-based outphasing power amplifier in 40-nm CMOS with 49.2% efficiency and 22.2 dBm power,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 206–209.
- [40] J. Chen *et al.*, “A digitally modulated mm-wave Cartesian beamforming transmitter with quadrature spatial combining,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 232–233.
- [41] C. Liang and B. Razavi, “Transmitter linearization by beamforming,” *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1956–1969, Sep. 2011.
- [42] D. A. Calvillo-Cortes *et al.*, “A package-integrated chireix outphasing RF switch-mode high-power amplifier,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3721–3732, Oct. 2013.
- [43] T. W. Barton and D. J. Perreault, “Four-way microstrip-based power combining for microwave outphasing power amplifiers,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2987–2998, Oct. 2014.
- [44] T. W. Barton and D. J. Perreault, “Theory and implementation of RF input outphasing power amplification,” *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4273–4283, Dec. 2015.

- [45] H. Wang *et al.*, *Power Amplifiers Performance Survey 2000-Present*. Accessed: Nov. 23, 2018. [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html
- [46] O. Momeni and E. Afshari, “High power terahertz and millimeter-wave oscillator design: A systematic approach,” *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.
- [47] M. Huang, T. Chi, S. Li, T. Huang and H. Wang, “A 24.5–43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO,” *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1177-1186, May 2020.
- [48] S. Li, T. Chi, T. Huang, M. Huang, D. Jung, and H. Wang, “A bufferless wideband frequency doubler in 45-nm CMOS-SOI with transistor multiport waveform shaping achieving 25% drain efficiency and 46– 89 GHz instantaneous bandwidth,” *IEEE Solid-State Circuits Lett.*, vol. 2, no. 4, pp. 25–28, Apr. 2019.
- [49] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Chichester, U.K.: Wiley, 2006.
- [50] S. Golar, S. Moloudi, and A. A. Abidi, “Processes of AM-PM distortion in large-signal single-FET amplifiers,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 245–260, Feb. 2017.
- [51] H. Wang *et al.*, “Towards Energy-Efficient 5G Mm-Wave links: Exploiting broadband Mm-Wave doherty power amplifier and multi-feed antenna with direct on-antenna power combining,” in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2017, pp. 30-37.
- [52] H. Wang *et al.*, “Broadband, linear, and high-efficiency mm-Wave PAs in silicon—Overcoming device limitations by architecture/circuit innovations,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1122–1125.
- [53] D. Jung, J. Park, S. Li, T. Huang, H. Zhao and H. Wang, “A 1.2 V Single Supply Hybrid Current-/Voltage-Mode Three-Way Digital Doherty PA with Built-In Large-Signal Phase Compensation Achieving Less-Than 5° AM-PM,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 2019, pp. 1-4.
- [54] D. Jung, S. Li, J. Park, T. Huang, H. Zhao and H. Wang, “A CMOS 1.2-V Hybrid Current- and Voltage-Mode Three-Way Digital Doherty PA With Built-In Phase Nonlinearity Compensation,” *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 525-535, March 2020.
- [55] H. T. Nguyen, T. Chi, S. Li and H. Wang, “A linear high-efficiency millimeter-wave CMOS Doherty radiator leveraging multi-feed on- antenna active load modulation,” *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3587-3598, Dec. 2018.

- [56] H. T. Nguyen, S. Li and H. Wang, "A mm-Wave 3-Way Linear Doherty Radiator with Multi Antenna Coupling and On-Antenna Current-Scaling Series Combiner for Deep Power Back-Off Efficiency Enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 84-86.
- [57] F. Wang, T. Li, S. Hu and H. Wang, "A Super-Resolution Mixed-Signal Doherty Power Amplifier for Simultaneous Linearity and Efficiency Enhancement," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3421-3436, Dec. 2019.
- [58] T. Li, M. Huang and H. Wang, "Millimeter-Wave Continuous-Mode Power Amplifier for 5G MIMO Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 7, pp. 3088-3098, July 2019.
- [59] N. S. Mannem, M. Huang, T. Huang, S. Li and H. Wang, "A Reconfigurable Series/Parallel Quadrature-Coupler-Based Doherty PA in CMOS SOI with VSWR Resilient Linearity and Back-Off PAE for 5G MIMO Arrays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 364-366.
- [60] S. Li, T. Chi, J. Park, H. T. Nguyen and H. Wang, "A 28-GHz Flip-Chip Packaged Chireix Transmitter with On-Antenna Outphasing Active Load Modulation," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1243-1253, May 2019.
- [61] T. W. Barton and D. J. Perreault, "An RF-input outphasing power amplifier with RF signal decomposition network," in *Proc. IEEE MTT-S Int. Microw. Symp.*, May 2015, pp. 1-4.
- [62] T. W. Barton and D. J. Perreault, "Theory and Implementation of RF-Input Outphasing Power Amplification," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 12, pp. 4273-4283, Dec. 2015.
- [63] H. Jang *et al.*, "RF-Input Self-Outphasing Doherty-Chireix Combined Amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 12, pp. 4518-4534, Dec. 2016.
- [64] D. N. Martin, T. Cappello, M. Litchfield and T. W. Barton, "An X-band RF-input outphasing power amplifier," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Jun. 2018, pp. 308-311.
- [65] B. Rabet and P. M. Asbeck, "A 28 GHz Single-Input Linear Chireix (SILC) Power Amplifier in 130 nm SiGe Technology," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 6, pp. 1482-1490, June 2020.
- [66] K. Ning, Y. Fang, N. Hosseinzadeh and J. F. Buckwalter, "A 30-GHz CMOS SOI outphasing power amplifier with current mode combining for high backoff efficiency and constant envelope operation," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1411-1421, May 2020.

- [67] S. Li, M. Huang, D. Jung, T. Huang and H. Wang, "A 28GHz Current-Mode Inverse-Outphasing Transmitter Achieving 40%/31% PA Efficiency at Psat/6dB PBO and Supporting 15Gbit/s 64-QAM for 5G Communication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 366-368.
- [68] R. King and Tai Wu, "The cylindrical antenna with arbitrary driving point," *IEEE Trans. Antennas Propag.*, vol. 13, no. 5, pp. 710-718, Sep. 1965.
- [69] R. Harrington and J. Mautz, "Straight wires with arbitrary excitation and loading," *IEEE Trans. Antennas Propag.*, vol. 15, no. 4, pp. 502-515, July 1967.
- [70] P. Fanson, Kun-Mu Chen, "Modification of antenna radiating characteristics with multi-impedance loading," *IEEE Trans. Antennas Propag.*, vol. 21, no. 5, pp. 715-721, 1973.
- [71] S. Jia, W. Chen and D. Schreurs, "A Novel Doherty Transmitter Based on Antenna Active Load Modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 4, pp. 271-273, Apr. 2015.
- [72] J. R. Copeland, W. J. Roberston, R. G. Verstraete, "Antennafier arrays," *IEEE Trans. Antennas Propag.*, vol. 12, no. 2, pp. 227-233, Mar. 1964.
- [73] M. L Kontorovich, N. M. Lyapunova, "Active antennas," *Radio Eng. Electron. Phys.*, vol. 19, pp. 126-127, 1974.
- [74] J. A. Navarro, K. A. Hummer, K. Chang, "Active integrated antenna elements," *Microwave J.*, vol. 34, pp. 115-126, Jan. 1991.
- [75] Jenshan Lin and T. Itoh, "Active integrated antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 42, no. 12, pp. 2186-2194, Dec. 1994.
- [76] K. Chang, R. A. York, P. S. Hall and T. Itoh, "Active integrated antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 937-944, March 2002.
- [77] S. M. Bowers and A. Hajimiri, "Multi-port driven radiators," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no 12, pp 4428-4441, Dec. 2013.
- [78] S. M. Bowers, A. Safaripour, and A. Hajimiri, "An integrated slot-ring traveling-wave radiator," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1154–1162, Apr. 2015.
- [79] K. Sengupta and A. Hajimiri, "Distributed active radiation for THz signal generation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 288–289.

- [80] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013-3031, Dec. 2012.
- [81] B. Abiri and A. Hajimiri, "A 69-to-79GHz CMOS multiport PA/radiator with +35.7dBm CW EIRP and integrated PLL," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 404-406.
- [82] O. A. Iupikov *et al.*, "A dual-fed PIFA antenna element with nonsymmetric impedance matrix for high-efficiency Doherty transmitters: integrated design and OTA-characterization," *IEEE Trans. on Antennas Propag.*, vol. 68, no. 1, pp. 21-32, Jan. 2020.
- [83] S. Lee, M. E. D. Smith, S. Li and H. Wang, "An Ultra-Wideband Edge-Fed Octagonal Four-Arm Archimedean Spiral Antenna," in *Proc. IEEE Int. Symp. Antennas Propag.*, Jun. 2019, pp. 207-208.
- [84] T. Chi, J. S. Park, S. Li and H. Wang, "A 64GHz full-duplex transceiver front-end with an on-chip multifeed self-interference-canceling antenna and an all-passive canceler supporting 4Gb/s modulation in one antenna footprint," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 76-78.
- [85] T. Chi, J. S. Park, S. Li and H. Wang, "A millimeter-wave polarization-division-duplex transceiver front-end with an on-chip multifeed self-interference-canceling antenna and an all-passive reconfigurable canceller," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3628-3639, Dec. 2018.
- [86] T. Chi, H. Wang, M.-Y. Huang, F. F. Dai, H. Wang, "A bidirectional lens-free digital-bits-in/-out 0.57mm² Terahertz nano-radio in CMOS with 49.3mW peak power consumption supporting 50cm Internet-of-Things communication," in *Proc. IEEE Custom Integr. Circuits Conf.*, pp. 1-4, 2017.
- [87] S. Li *et al.*, "An E-band high-linearity antenna-LNA frontend with 4.8 dB NF and 2.2 dBm IIP3 exploiting multi-feed on-antenna noise-canceling and gm-boosting", in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 1-3.
- [88] S. Li *et al.*, "Performance of V-band on-chip antennas in GlobalFoundries 45nm CMOS SOI process for mm-wave 5G applications," in *Proc. IEEE MTT-S Int. Microw. Symp.*, June 2018, pp. 1593-1596.
- [89] F. Bruccoleri, E. A. M. Klumperink and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275-282, Feb. 2004.

- [90] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband noise-canceling CMOS LNA exploiting a transformer," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2006, pp. 137-140.
- [91] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, June 2008.
- [92] Q. Zhong, W. Choi, C. Miller, R. Henderson and K. K. O, "A 210-to-305GHz CMOS receiver for rotational spectroscopy," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 426-427.
- [93] C. Wang and R. Han, "Rapid and energy-efficient molecular sensing using dual mm-Wave combs in 65nm CMOS: A 220-to-320GHz spectrometer with 5.2mW radiated power and 14.6-to-19.5dB noise figure," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 302-303.
- [94] C. T. Coen *et al.*, "Design and on-wafer characterization of G-band SiGe HBT low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3631-3642, Nov. 2016.
- [95] F. Ulaby *et al.*, *Microwave Remote Sensing: Active and Passive*, vol. 1. Dedham, MA: Artech House, 1986.
- [96] B. Rupakula and G. M. Rebeiz, "Third-Order Intermodulation Effects and System Sensitivity Degradation in Receive-Mode 5G Phased Arrays in the Presence of Multiple Interferers," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5780-5795, Dec. 2018.